datasheet

PRELIMINARY SPECIFICATION

1/2.9" color CMOS 1080p (1920 x 1080) high dynamic range (HDR) high definition (HD) image sensor

OV2718

color CMOS 1080p (1920x1080) high dynamic range (HDR) high definition image sensor

datasheet (CSP)
PRELIMINARY SPECIFICATION

version 1.0
january 2017

To learn more about OmniVision Technologies, visit www.ovt.com.

applications

- security and surveillance cameras
- video applications
- smart home

ordering information

- **OV02718-H77A-2A** (color, lead-free) 77-pin CSP
- **OV02718-H77A-PA** (color, lead-free) 77-pin CSP with protective film

note Since it is impossible to check compatibility with all displays, check the interoperability before committing to mass production.

features

- support for image size: 1920x1080, VGA, QVGA, and any cropped size
- high dynamic range
- high sensitivity
- low power consumption
- image sensor processor functions: lens correction, defective pixel cancelation, and automatic black level correction
- supported output formats: RAW
- horizontal and vertical sub-sampling
- SCCB for register programming
- high speed serial data transfer with MIPI CSI-2/LVDS
- parallel 12-bit DVP output
- external frame synchronization capability
- one time programmable (OTP) memory

note To reduce image artifacts from Infrared light, and provide the best image quality, OmniVision recommends an IR cut filter

key specifications (typical)

- **active array size:** 1920 x 1080
- **power supply:**
  analog: 3.14 ~ 3.47V
  digital: 1.2 ~ 1.4V
  DOVDD: 1.7 ~ 1.9V
  AVDD: 1.7 ~ 1.9V
- **power requirements:**
  active: 350 mW
  standby: 1.14 mW
- **temperature range:**
  operating: -30°C to 85°C junction temperature (see **table 8-2**)
  stable image: 0°C to +60°C junction temperature (see **table 8-2**)
- **output interfaces:** up to 4-lane MIPI CSI-2/LVDS, 12-bit DVP
- **input clock frequency:** 6 ~ 36 MHz
- **lens size:** 1/2.9"
- **lens chief ray angle:** 9° (see **figure 10-2**)
- **output formats:** linear - 12 bit RAW; HDR - 2x12 bit DCG RAW, 16 bit combined DCG, 12 bit compressed combined DCG
- **scan mode:** progressive
- **shutter:** rolling shutter
- **maximum image transfer rate:** 30 fps full resolution HDR, 30 fps full resolution linear
- **sensitivity:** 26200 e/lux.sec @ 530 nm
- **max S/N ratio:** 42.6 dB
- **dynamic range:** 120 dB
- **pixel size:** 2.8 µm x 2.8 µm
- **dark current:** 16 e^-/s
- **image area:** 5482.35 µm x 3202 µm
- **package dimensions:** 6534 µm x 5724 µm

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1 application system

1.1 overview

The OV2718 color image sensor is a 1/2.9" optical format, 1920x1080 single-chip, low power CMOS, active-pixel digital high dynamic range sensor for high end 1080p security market.

The OV2718 features OmniBSI-2™ technology to extend the dynamic range. The sensor supports dual conversion gain (DCG) with 90 dB dynamic range.

The OV2718 performs sophisticated camera functions on-chip controlled via the SCCB interface. These functions include lens shading correction, dual conversion gain (DCG) combination, and defect pixel correction. The OV2718 enables advanced HDR imaging in a simple, cost effective system.

1.2 signal description and pin assignment

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV2718 image sensor. The package information is shown in **section 9**.

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	NC	–	no connect
A3	DOGND	ground	ground for I/O and digital circuit
A4	DVDD	power	digital circuit power
A5	NC	–	no connect
A6	NC	–	no connect
A7	NC	–	no connect
A8	DVDD	power	digital circuit power
A9	NC	–	no connect
A10	NC	–	no connect
B1	NC	–	no connect
B2	AGND	ground	analog ground
B3	AVDD18	power	analog power
B4	AVDD_LO	power	analog power
B5	NC	–	no connect
B6	NC	–	no connect
B7	NC	–	no connect
B8	NC	–	no connect
B9	DOGND	ground	ground for I/O and digital circuit
B10	NC	–	no connect
C1	SVDD_PIX	power	sensor power (pixel array)
C2	SVDD_PIX_CAP	power	SVDD_PIX capacitor connection
C3	SVDD	power	sensor power
C4	NC	–	no connect
C6	NC	–	no connect

table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
C7	NC	–	no connect
C8	NC	–	no connect
C9	NC	–	no connect
C10	NC	–	no connect
D1	HVDD2_CAP	analog I/O	HVDD2 capacitor connection
D2	HVDD2	analog I/O	HVDD2 regulated supply
D3	**PWDNB**	input	power down (active low with pull up resistor)
D4	ATEST	analog I/O	analog test I/O
D7	NC	–	no connect
D8	NC	–	no connect
D9	DOVDD	power	I/O power
D10	**GPIO0/FSIN**	I/O	general purpose I/O/frame sync input
E1	NVDD	analog I/O	NVDD regulated supply
E2	DOVDD	power	I/O power
E3	**MDP2/D0**	output	MIPI_LVDS data output/DVP data output
E4	**MDP0/D2**	output	MIPI_LVDS data output/DVP data output
E5	**MCP/D4**	output	MIPI_LVDS clock output/DVP data output
E6	**MDP1/D6**	output	MIPI_LVDS data output/DVP data output
E7	**MDP3/D8**	output	MIPI_LVDS data output/DVP data output
E8	**TM**	input	test mode (active high with pull down resistor)
E9	**SCL**	input	SCCB interface input clock
E10	DOGND	ground	ground for I/O and digital circuit
F1	DVDD	power	digital circuit power
F2	DOGND	ground	ground for I/O and digital circuit
F3	**MDN2/D1**	output	MIPI_LVDS data output/DVP data output
F4	**MDN0/D3**	output	MIPI_LVDS data output/DVP data output
F5	**MCN/D5**	output	MIPI_LVDS clock output/DVP data output
F6	**MDN1/D7**	output	MIPI_LVDS data output/DVP data output
F7	**MDN3/D9**	output	MIPI_LVDS data output/DVP data output
F8	**HREF**	output	video output horizontal signal

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
F9	**SDA**	I/O	SCCB interface data pin
F10	**RESETB**	input	reset/power down (active low with pull up resistor)
G1	**XVCLK**	input	clock input
G2	PVDD	power	PLL power supply
G3	DOGND	ground	ground for I/O and digital circuit
G4	EVDD	power	digital circuit power
G5	EVDD	power	digital circuit power
G6	DOGND	ground	ground for I/O and digital circuit
G7	**D10**	output	DVP data output
G8	**GPIO1/VSYNC**	I/O	general purpose I/O/video output vertical signal
G9	DVDD	power	digital circuit power
G10	NC	–	no connect
H1	NC	–	no connect
H2	**PCLK**	I/O	DVP clock input
H3	DOVDD	power	I/O power
H4	EVDD	power	digital circuit power
H5	EVDD	power	digital circuit power
H6	DOVDD	power	I/O power
H7	**D11**	output	DVP data output
H8	DOGND	ground	ground for I/O and digital circuit
H9	NC	–	no connect
H10	NC	–	no connect

table 1-2 pin states under various conditions

pin number	signal name	RESETB = 0	RESETB = 1 PWDNB = 1 stream/standby	RESETB = 1 PWDNB = 0 hardware standby/power down
D3	PWDNB	input	input	input
D10	GPIO0/FSIN	input	input (configurable)[c]	input (configurable)[c]
E3	MDP2/D0	output[a]	output (configurable)[b]	output (configurable)[b]
E4	MDP0/D2	output[a]	output (configurable)[b]	output (configurable)[b]
E5	MCP/D4	output[a]	output (configurable)[b]	output (configurable)[b]
E6	MDP1/D6	output[a]	output (configurable)[b]	output (configurable)[b]
E7	MDP3/D8	output[a]	output (configurable)[b]	output (configurable)[b]
E8	TM	input	input	input
E9	SCL	input	input	input
F3	MDN2/D1	output[a]	output (configurable)[b]	output (configurable)[b]
F4	MDN0/D3	output[a]	output (configurable)[b]	output (configurable)[b]
F5	MCN/D5	output[a]	output (configurable)[b]	output (configurable)[b]
F6	MDN1/D7	output[a]	output (configurable)[b]	output (configurable)[b]
F7	MDN3/D9	output[a]	output (configurable)[b]	output (configurable)[b]
F8	HREF	output[a]	output (configurable)[b]	output (configurable)[b]
F9	SDA	open-drain	open-drain	open-drain
F10	RESETB	input	input	input
G1	XVCLK	input	input	input
G7	D10	output[a]	output (configurable)[b]	output (configurable)[b]
G8	GPIO1/VSYNC	input	input (configurable)[c]	input (configurable)[c]
H2	PCLK	output[a]	output (configurable)[b]	output (configurable)[b]
H7	D11	output[a]	output (configurable)[b]	output (configurable)[b]

a. tri-stated

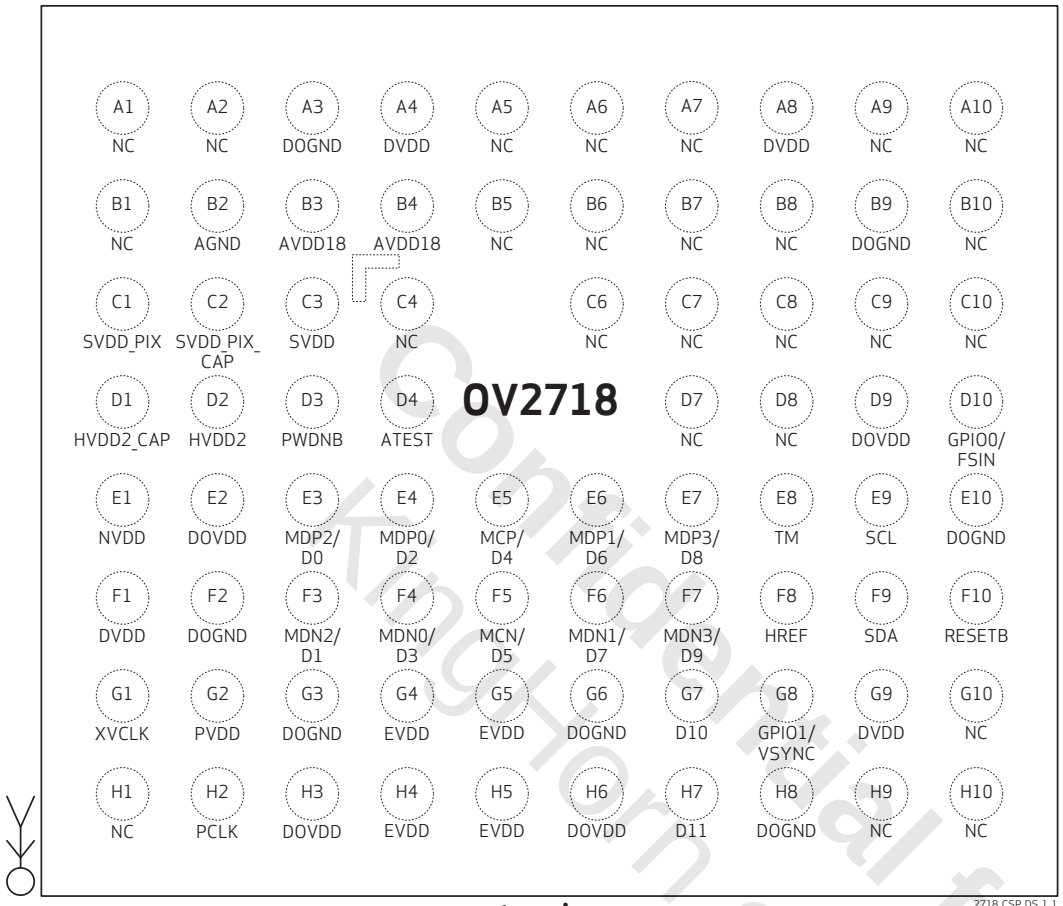
b. 0x3488[5]: drive-value, 0x3488[4]: drive enable

c. see **table 1-3**

table 1-3 GPIO control registers

address	register name	default value	R/W	description
0x3489	GPIO_OE	0x00	RW	GPIO Output Enable Bit[1]: GPIO1 output enable Bit[0]: GPIO0 output enable
0x348A	GPIO_O	0x00	RW	GPIO Output Value Bit[1]: GPIO1 output value Bit[0]: GPIO0 output value
0x348B	GPIO_CTRL	0x04	RW	Bit[7:5]: gpio_sel0 001: Row trigger 010: Not used 011: Not used 100: PLL1 lock 101: PLL2 lock 110: Watchdog pulse Bit[4:3]: gpio_sel1 01: VSYNC 10: Not used 11: Sequencer GPIO1

figure 1-1 pin diagram



top view
(bumps down)

table 1-4 pad equivalent circuit (sheet 1 of 2)

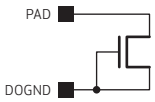
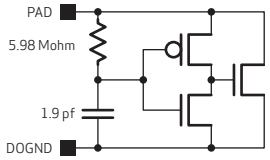
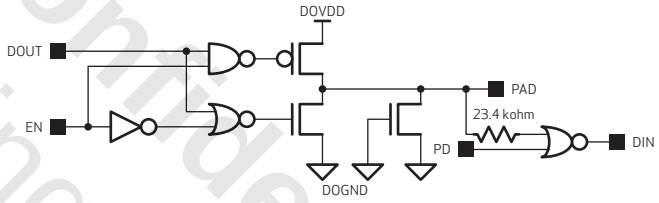
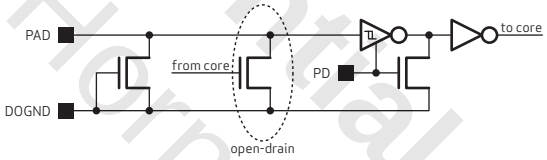
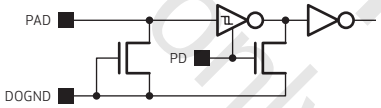
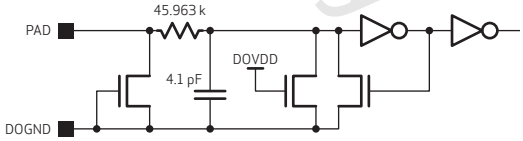
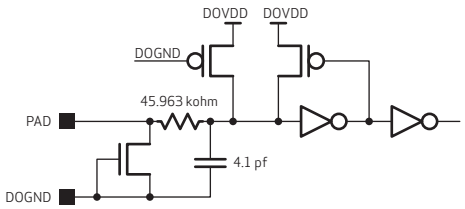
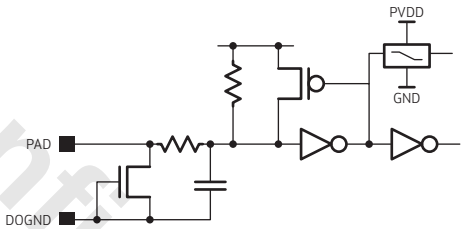
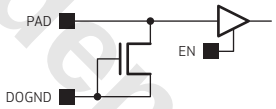
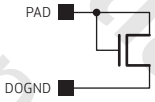
signal name	equivalent circuit
DOGND, DOVDD, HVDD2_CAP, HVDD2, ATEST, SVDD_PIX_CAP, SVDD_PIX, AGND, AGND_PIX	
DVDD, SVDD, PVDD, AVDD18, EVDD, AVDD_LO	
GPIO0/FSIN, GPIO1/VSYNC, HREF, D10, D11, MDN3/D9, MDP3/D8, MDN1/D7, MDP1/D6, MCN/D5, MCP/D4, MDN0/D3, MDP0_D2, MDN2/D1, MDP2/D0, PCLK	
SDA	
SCL	
TM	

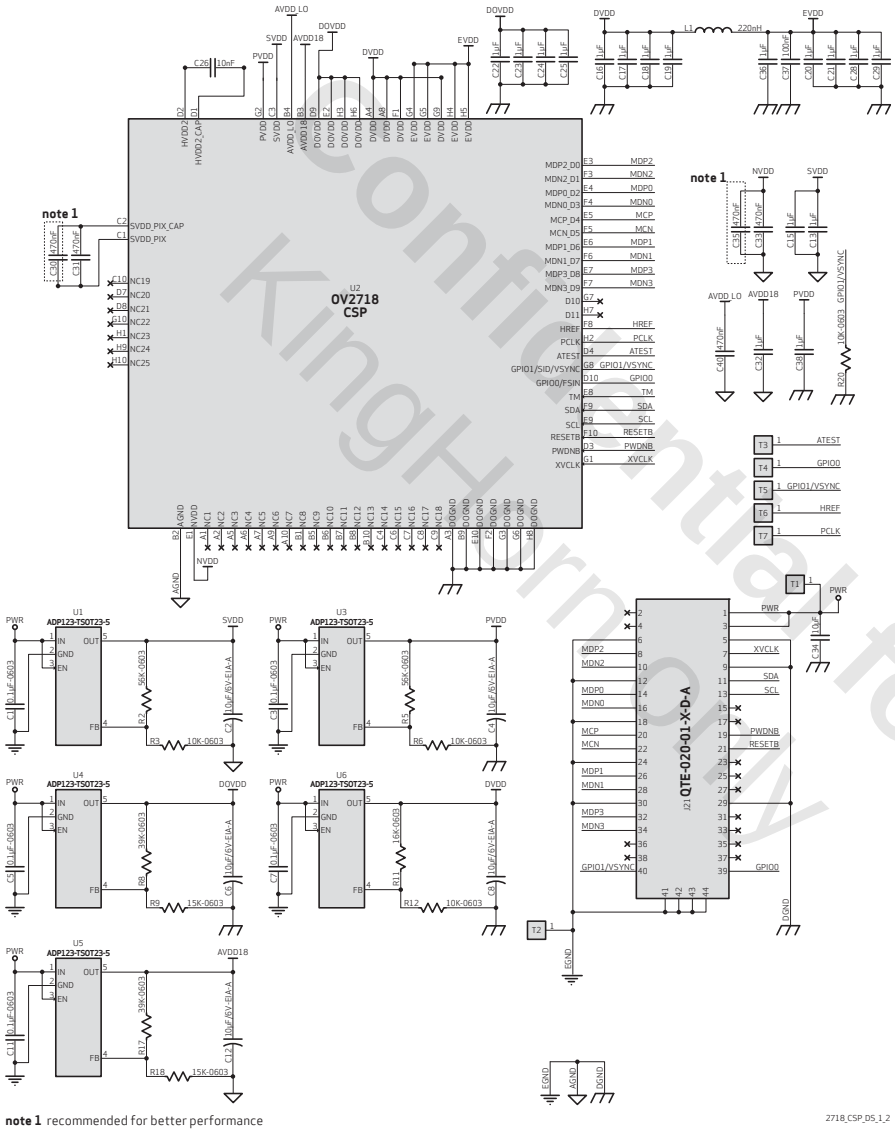
table 1-4 pad equivalent circuit (sheet 2 of 2)

signal name	equivalent circuit
RESETB	
PWDNB	
XVCLK	
NVDD	

1.3 reference design

The silicon revision can be read from register 0x300D. **figure 1-2** shows the power supply and signal connection of the OV2718 when using MIPI interface. The SCCB ID will be defined by voltage level of GPIO1 at power up, after hardware reset (RESETB pin low) and after software reset (0x3013[0]=1): "6C" by default or defined by 0x300C when GPIO1 has a pull-down resistor; "20" when GPIO1 has a pull-up resistor, which is hard coded and cannot be changed.

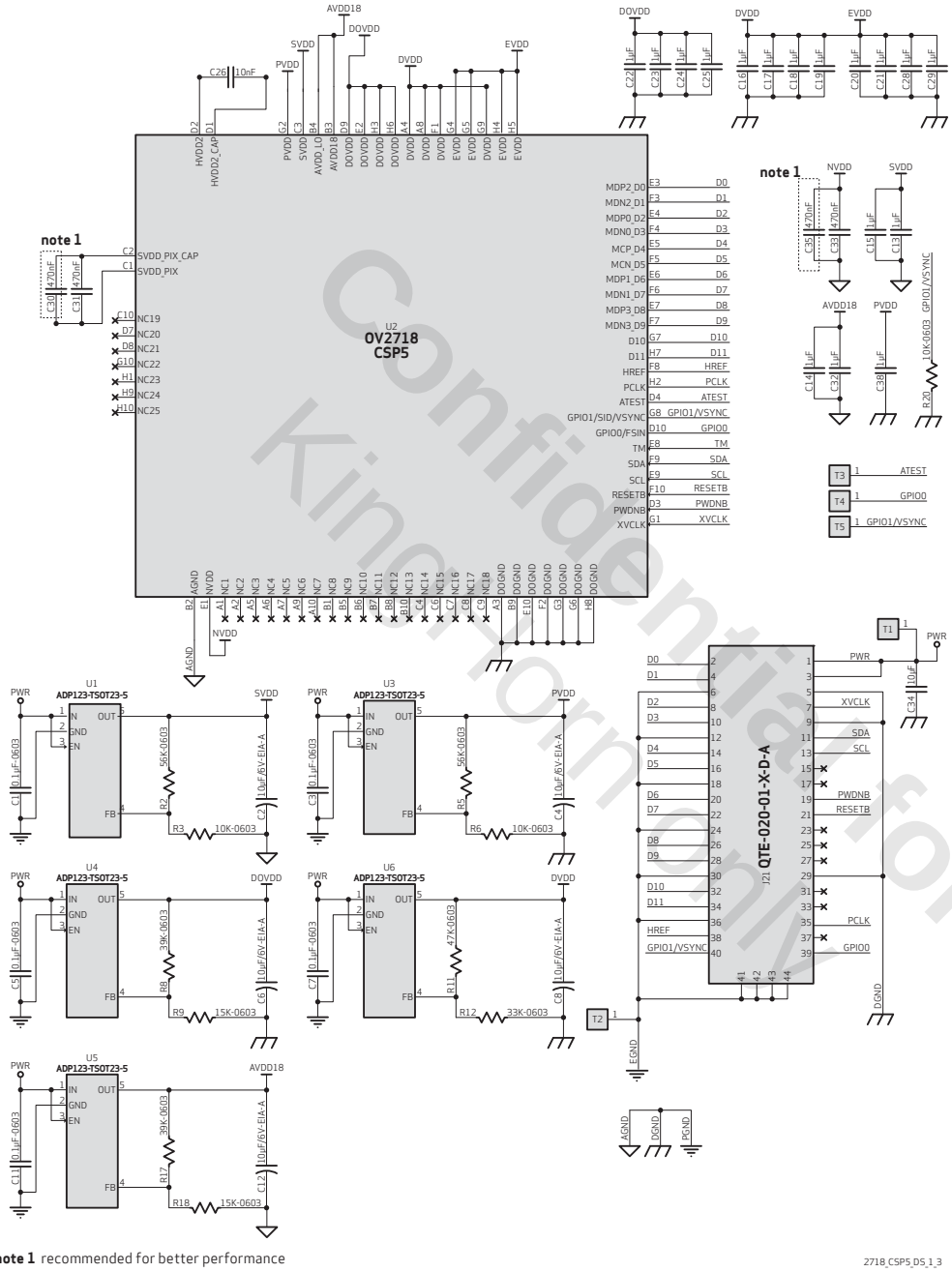
figure 1-2 OV2718 MIPI reference schematic



note 1 recommended for better performance

figure 1-3 shows the power supply and signal connection of the OV2718 when using DVP interface.

figure 1-3 OV2718 DVP reference schematic



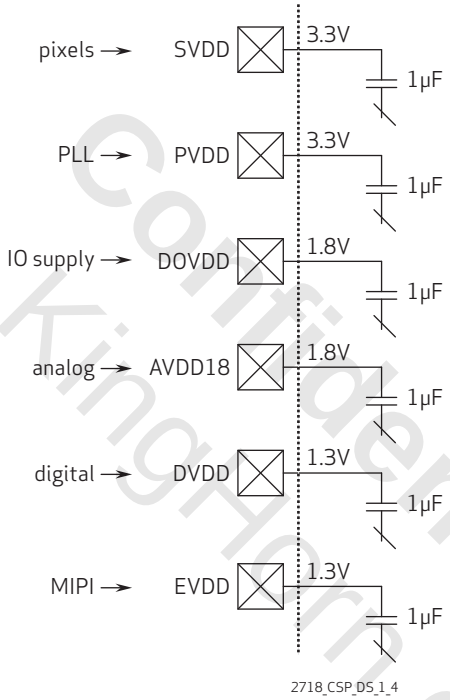
note 1 recommended for better performance

2718_CSP5_DS_1_3

1.3.1 external components

The pixel array is powered from 3.3V (SVDD). Analog supply is 1.8V (AVDD18). I/O pad power (DOVDD) is 1.8V. Core logic operates on 1.3V (DVDD). The high speed serial MIPI interface is supplied from 1.3V (EVDD). The OV2718 must use external power de-coupling capacitors to reduce noise. The default capacitor value is 1µF. At power up, the power supplies should ramp up in 50 µs or more to avoid in-rush current during ramp-up.

figure 1-4 OV2718 power supplies and recommended external decoupling

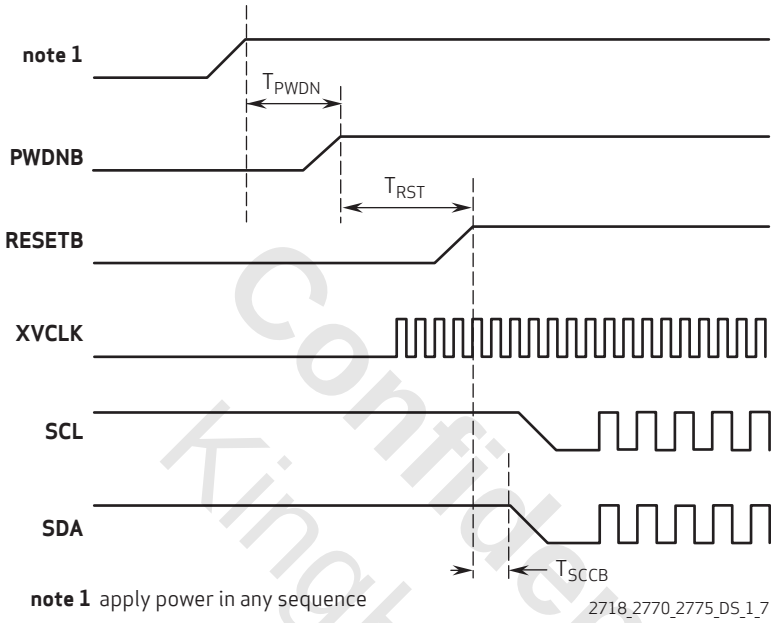


1.3.2 power on reset (POR) generation

Reset can be controlled from the external pin. However, inside this chip, there is a power on reset generation function to auto detect core power at stable state.

1.4 power up sequence/ boot sequence

figure 1-5 power on timing diagram



When power is applied to the chip, the analog POR module keeps the chip in reset mode until the voltage is high enough to start operation. When the analog POR is released, an additional 9500 XVCLK cycles are used to give some extra time for the system to stabilize (e.g., load OTP memory). To extend this period, keep the RESETB pin low. The chip will then enter software reset state (SW_RESET). SW_RESET can also be reached by any other state by writing the software reset bit over SCCB.

T_{SCCB} starts from RESETB going high or when XVCLK is present, whichever is last. The XVCLK must be stable before reset mode is released since reset mode release is clocked by XVCLK. When it is finished, the standby state is reached and the sensor can be programmed over SCCB.

table 1-5 power on timing

parameter	min	max	unit
T_{PWDN}	1	n/a	ms
T_{RST}	0	n/a	ms
T_{SCCB}	9500	n/a	XVCLK cycles

1.4.1 power down sequence

When in standby mode, power down mode can be entered by pulling the PWDNB pin low. In this state, all internal clocks are gated and the internal regulator is set in a power-saving low-power mode. When the regulator resumes from low power mode 32767 XVCLK cycles are waited before turning on any clocks to ensure safe operation. The power down mode can only be entered from the standby mode.

1.4.2 operating modes

A software reset is required to reset all registers back to their default values. Set register 0x3013[0] and the sensor will be in standby mode after the software reset. It is highly recommended to wait 10ms before programming other registers after a software reset.

The OV2718 supports the following modes:

- reset mode
  - enabled when RESETB pin low
  - all modules brought to reset, including registers
  - IOs tri-stated
  - no active clocks
  - disabled SCCB
- power down mode (suspend mode)
  - enabled when PWDNB pin low
  - register values are not maintained
  - IOs de-activated (can be tri-stated or driven high or low by register control)
  - clock input is blocked to internal circuit logic control
  - internal clocks stopped
  - all sensor modules powered off, including SCCB
- standby mode
  - asserted after power-up and after SCCB command register 0x3012[0]=0
  - all modules powered ON
  - pads are active
  - PLL stopped (if early activation is not enabled)
- streaming mode
  - image capture and output streaming enabled

1.4.3 activation sequence

In standby mode, by setting register 0x3012[0]=0; and in streaming mode, by setting register 0x3012[0]=1, the necessary analog modules and the PLLs are turned on. When the PLLs are stable after 4096 XVCLK cycles, the main clocks are switched from XVCLK to the faster PLL clock. When Tinit is done, streaming is activated.

1.4.4 deactivation sequence

In streaming mode, by clearing register 0x3012[0], the chip will enter standby after finishing the current frame (finish is signaled by VSYNC at the DVP-FIFO). The main clock is switched from PLL to XVCLK clock. If early activation is not set, PLLs and analog modules are turned off. To further reduce the power consumption from the standby state, the PWDNB pin can be pulled low. When this pin is low, the chip is not accessible through SCCB.

All registers are reset to default values by writing the software reset bit over SCCB. It is highly recommended to wait 10ms before programming other registers after a software reset.

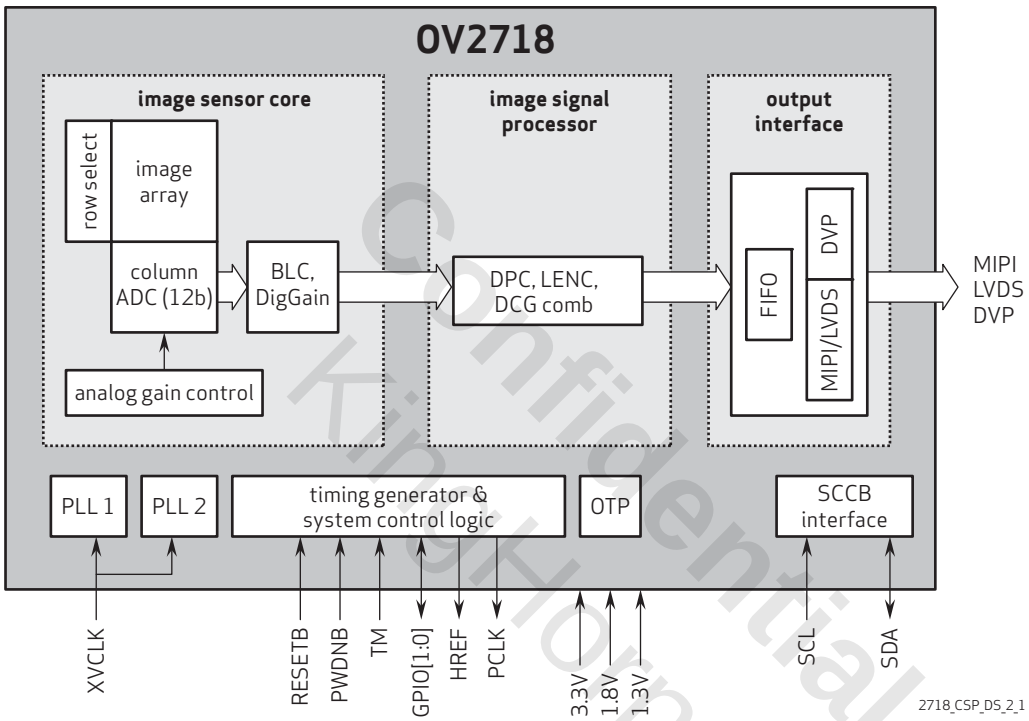
1.4.5 early activation

For faster activation, the user can choose to power up the analog modules and PLLs in standby mode. Since the PLLs are dependent on the analog to be powered up, register 0x3014[2] must be set to turn on the analog modules and for early PLL startup to work. Early PLL startup is enabled by setting register 0x3014[1].

2 sensor architecture

figure 2-1 shows the top level block diagram of the OV2718 sensor.

figure 2-1 OV2718 block diagram



The sensor consists of three major functional blocks: image sensor core, image signal processor (ISP), and output interface.

The image sensor core receives the photo signal which generates electrical charge collected by the pixel photo diodes (PDs). During readout, the accumulated charge is converted to a voltage signal in the pixel. This signal is then amplified and converted to a digital signal by the analog-to-digital converter (ADC). Dark current and circuit offsets are compensated by the black level correction circuit (BLC). The correction is implemented purely in the digital domain. Dark current increases exponentially with temperature and the BLC can be configured to automatically re-trigger with changes in junction temperature, in addition to changes in gain.

The OV2718 offers dual conversion gain (DCG) HDR, which means switchable two conversion gain (CG) in one exposure (integration time) - low conversion gain (LCG) for large charge handling capacity in bright scenes and a high conversion gain (HCG) mode with increased sensitivity and low read noise for low-light scenes. Higher CG means higher sensitivity, as one signal electron can be more easily detected. Higher CG also means that the sensor will realize a reduction in read noise. The output from the HCG and LCG channels are combined in the sensor to create a 90 db (16-bit) HDR output image. The ISP also supports lens correction (LENC) and defect pixel correction (DPC).

The processed linear or combined HDR image is formatted and output through the digital video port (DVP) interface or the MIPI/LVDS interface. Two on-chip phase lock loops (PLLs) generate the required clock signals for all blocks from the XVCLK input clock. The timing generator generates the control signals for the pixel array to reset the PD at the beginning of the exposure, to stop the exposure by reading out the accumulated charge, and also to generate the required control timing for the readout amplifier and ADC. In DVP mode, the horizontal synchronization reference (HREF), vertical synchronization (VSYNC, which can be configured to the GPIO pad), and pixel clock (PCLK) signals are also generated so the backend processor can receive the image data.

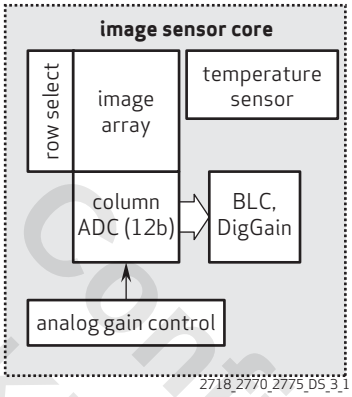
The one time programmable (OTP) memory contains the DPC value and temperature offset value, etc.

All functional blocks are controlled by registers. The host controller can program and read back through the SCCB interface.

3 image sensor core

figure 3-1 shows the top level block diagram of the OV2718 image sensor core.

figure 3-1 sensor core block diagram



The image sensor core consists of the active pixel array, row access control circuit, column parallel analog-to-digital converter (ADC) with gain control, and analog readout channel. A single analog readout channel is used for the processing of two capture channels (HCG, LCG). This provides optimal matching between the capture channels. Gain and BLC are implemented in digital domain.

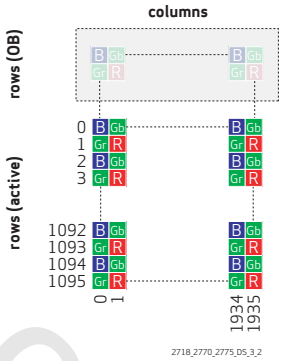
3.1 pixel array structure

The OV2718 sensor has an image array of 1936 columns by 1096 rows covered with color filters arranged in a Bayer pattern. **figure 3-2** shows the pixel array color filter layout. In addition to the active pixel rows, optical black (OB) pixel rows are embedded to serve as reference pixels for the black level correction (BLC). The OB rows are covered with a light shield (solid metal layer). In order to minimize non-ideal edge effects in the output image, it is not recommended to use the pixels at the lowest and highest row and column addresses.

The entire readable column: 1920 active columns + 8 active border columns (image quality guarantee) + 8 extra active border columns (no image quality guarantee) = 1936 column

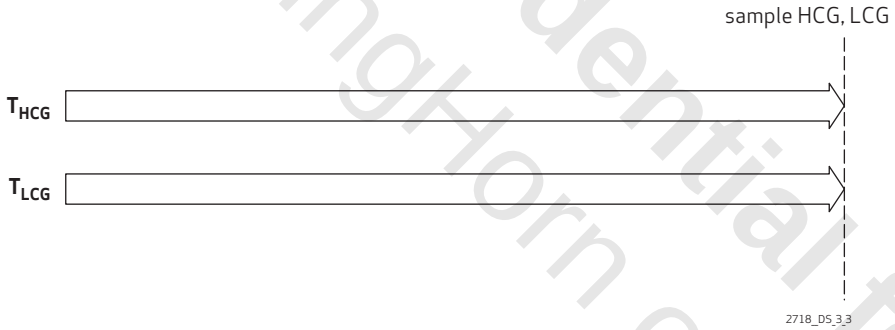
The entire readable row: 1080 active rows + 8 active border rows (image quality guarantee) + 8 extra active border rows (no image quality guarantee) = 1096 rows

figure 3-2 pixel array region color filter layout



Each pixel has two switchable conversion gains (CG) to extend the dynamic range. Higher CG (HCG) means higher sensitivity, as one signal electron can be more easily detected. Lower CG (LCG) means lower sensitivity. The integration time diagram is shown in **figure 3-3**.

figure 3-3 integration time diagram



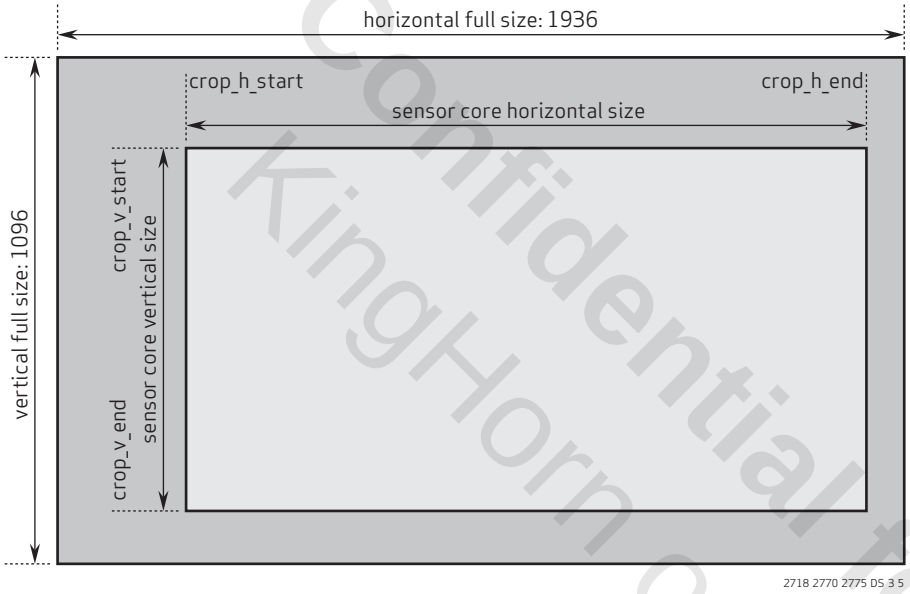
The OV2718 can operate in two modes:

- HDR mode: HDR mode with DCG exposures with HCG and LCG
- linear mode: linear mode using one capture (HCG or LCG) valid

3.2 pixel array access

The readout window is fully programmable from 256 to 1936 in steps of 4 (8 in sub-sampling) in the horizontal direction and 20 to 1096 in steps of 2 (4 in sub-sampling) in the vertical direction. Start address must be at an even row and column and end address must be at an odd row and column address in order to preserve the Bayer pattern order. The 'crop' address in registers 0x30A0~0x30A7 programs the sensor core readout window and can be set freely within the pixel array. The start address should always be an even number, while the end address should always be an odd number. The crop window is programmed larger than the processed output image resolution because the ISP uses extra rows and columns for the image processing algorithms (e.g., defect pixel correction).

figure 3-4 pixel array access diagram



3.3 mirror and flip

The pixel array can be accessed in the reverse order in column and row directions (i.e., the image can be horizontally mirrored and vertically flipped. Refer to **figure 3-5**. Image flip is controlled by register 0x30C0[3]. The image mirror setting is shown in **table 3-1**. The sensor needs to be in standby mode when implementing mirror or flip.

table 3-1 register setting for mirror

register name	register address	value
mirror	0x30C0[2]	1
odp_h_offs_l	0x30A9	1
odp_h_size_h, odp_h_size_l	0x30AC, 0x30AD	crop window size - 2
cfa_pattern	0x3252[0]	1

figure 3-5 horizontal mirror and vertical flip samples

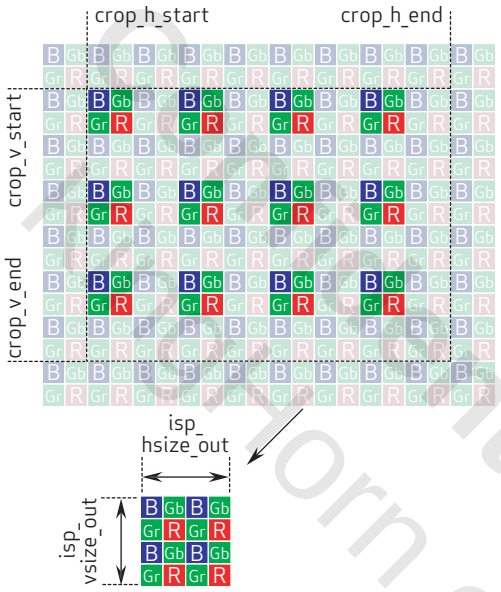
original image | mirrored image | flipped image | mirrored and flipped image

2718_2770_2775_DS_3_6

3.4 sub-sampling

The pixel array can be sub-sampled by a factor of 2 in both horizontal and vertical directions, controlled by register 0x30BF[1:0]. The sub-sampling is done in the sensor core. The ISP processes the output from the sensor core as a continuous stream of pixel values and generates a lower resolution output image. The horizontal and vertical sub-sampling can be programmed independently. The vertical sub-sampling enables a higher frame rate since the number of rows per frame is reduced, whereas the horizontal sub-sampling will not enable a higher frame rate since the number of clock periods per row is not reduced when horizontal sub sampling is enabled.

figure 3-6 horizontal and vertical sub-sampling



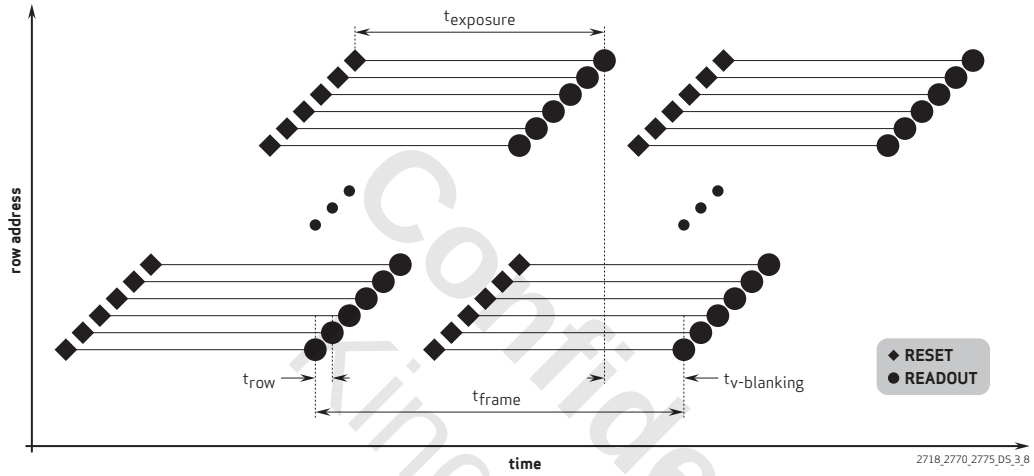
note when using sub-sampling, the size (crop_h_end - crop_h_st+1) and (crop_v_end - crop_v_st + 1) must be multiple of four

2718 2770 2775 DS 3 7

3.5 frame timing and maximum frame rate

The OV2718 employs an electronic rolling shutter (ERS) for exposure control (see **figure 3-7**). The pixel array is first reset row by row and when the exposure time has elapsed, the readout of the pixel array is done row by row.

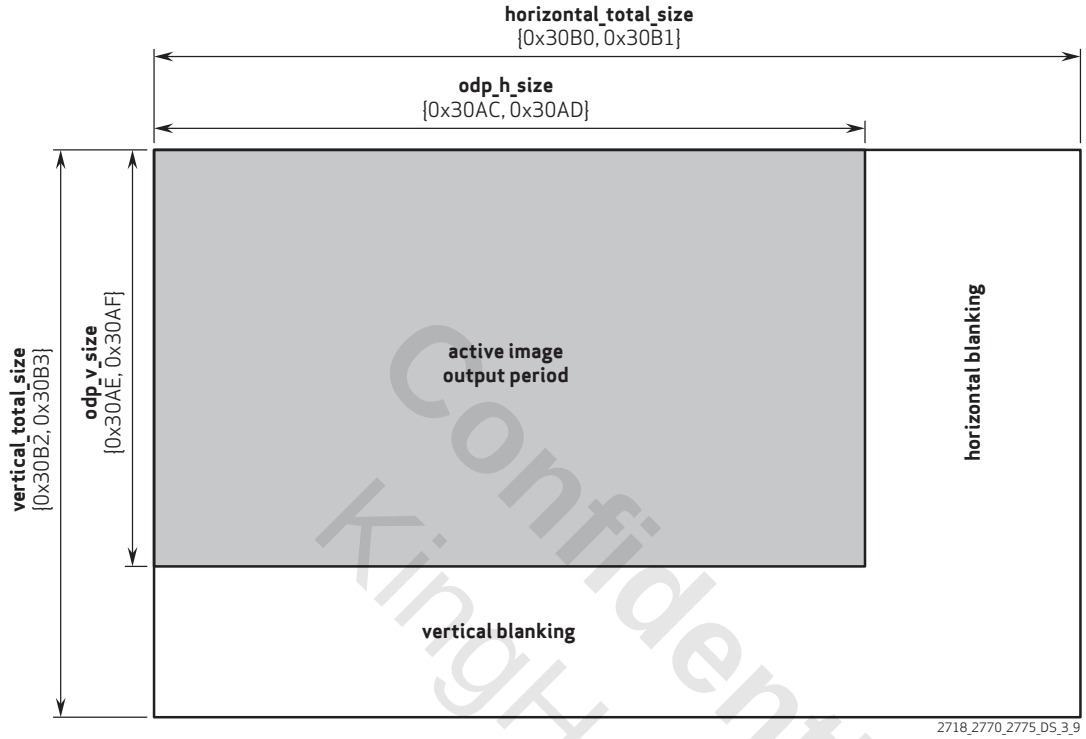
figure 3-7 row address versus time graph



The timing generator generates all the control signals based on a row counter and column counter. Refer to **figure 3-8** for the frame timing. The row period consists of an active output period and a horizontal blanking period. A vertical blanking period is also required to perform frame-based operation. The vertical blanking period seen by the backend processor is usually longer than the internal vertical blanking because the BLC is reading the optical black rows required to perform the correction.

A minimum number of clock periods are required to complete all the required operations per row (blanking time). Refer to **section 5** for details.

figure 3-8 frame output timing diagram



The maximum frame rate is determined by the maximum pixel clock, total number of pixels read out of the entire frame and minimum horizontal/vertical blanking time. The system clock and the minimum blanking time are usually fixed for a given design and the frame rate is dependent on the number of pixels read out. If the requested output image size (ODP size) is smaller than the full pixel array, it is not necessary to read out the whole pixel array, thus; the frame rate can be increased by cropping and/or sub-sampling the pixel array (see **figure** and **figure 3-6**). **table 3-2** and **table 3-3** list the most common image sizes and maximum frame rates that the sensor can achieve. Other image sizes are also possible by cropping and/or sub-sampling. Refer to **section 5** output interface for details.

table 3-2 supported output formats and frame rates for MIPI/LVDS

maximum frame rate supported via MIPI/LVDS(600 Mbps/lane) interface		
format		maximum frame rate
linear	12b	30 fps
HDR	2x12b DCG	30 fps
	16b combined DCG	30 fps
	12b compressed combined DCG	30 fps

table 3-3 supported output formats and frame rates for DVP

maximum frame rate supported via DVP (75 MHz) interface		
format		maximum frame rate
linear	12b	30 fps
HDR	12b compressed combined DCG	30 fps

table 3-4 timing control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x30A0	CROP_H_ST_H	0x00	RW	Start Address Horizontal High Byte
0x30A1	CROP_H_ST_L	0x00	RW	Start Address Horizontal Low Byte
0x30A2	CROP_V_ST_H	0x00	RW	Start Address Vertical High Byte
0x30A3	CROP_V_ST_L	0x00	RW	Start Address Vertical Low Byte
0x30A4	CROP_H_END_H	0x07	RW	End Address Horizontal High Byte
0x30A5	CROP_H_END_L	0x8F	RW	End Address Horizontal Low Byte
0x30A6	CROP_V_END_H	0x04	RW	End Address Vertical High Byte
0x30A7	CROP_V_END_L	0x47	RW	End Address Vertical Low Byte
0x30A8	ODP_H_OFFS_H	0x00	RW	Output Data Path Horizontal Offs High Byte
0x30A9	ODP_H_OFFS_L	0x00	RW	Output Data Path Horizontal Offs Low Byte
0x30AA	ODP_V_OFFS_H	0x00	RW	Output Data Path Vertical Offs High Byte
0x30AB	ODP_V_OFFS_L	0x00	RW	Output Data Path Vertical Offs Low Byte

table 3-4 timing control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x30AC	ODP_H_SIZE_H	0x07	RW	Output Data Path Horizontal Size High Byte
0x30AD	ODP_H_SIZE_L	0x90	RW	Output Data Path Horizontal Size Low Byte
0x30AE	ODP_V_SIZE_H	0x04	RW	Output Data Path Vertical Size High Byte
0x30AF	ODP_V_SIZE_L	0x4A	RW	Output Data Path Vertical Size Low Byte
0x30B0	HTS_H	0x09	RW	Line Length High Byte
0x30B1	HTS_L	0x98	RW	Line Length Low Byte
0x30B2	VTS_H	0x04	RW	Frame Length High Byte
0x30B3	VTS_L	0x65	RW	Frame Length Low Byte
0x30B4	EXTRA_DELAY_H	0x00	RW	(fs_delay) Last Row Can Be Extended by This Number of Clocks. Reset by sensor_ctrl.extra_ctrl
0x30B5	EXTRA_DELAY_L	0x00	RW	(fs_delay) Last Row Can Be Extended by This Number of Clocks. Reset by sensor_ctrl.extra_ctrl

In modes using on-chip combination, (ODP_V_OFFS_H, ODP_V_OFFS_L) must be set to zero and (ODP_V_SIZE_H, ODP_V_SIZE_L) must be equal to [(CROP_V_END_H, CROP_V_END_L) - (CROP_V_ST_H, CROP_V_ST_L) + 1].

3.6 exposure control

The OV2718 has one DCG exposure and two captures: (HCG and LCG). Their exposure time can be set manually in registers:

- Minimum exposure is one line. Maximum exposure is VTS -2 lines
- {0x30B6[7:0], 0x30B7[7:0]} for DCG (HCG and LCG) exposure time

All exposure time values are represented by the unit of row time.

$$\text{row time} = \frac{\text{HTS}}{\text{SCLK}}$$

where SCLK is the system clock and HTS is the horizontal total size {0x30B0, 0x30B1}.

The actual exposure time value of the current frame can be read back from 0x30C9[7:0]~0x30CA[7:0] for DCG (HCG and LCG).

table 3-5 exposure control registers

address	register name	default value	R/W	description
0x30B0	HTS_H	0x09	RW	Line Length High Byte
0x30B1	HTS_L	0x98	RW	Line Length Low Byte
0x30B2	VTS_H	0x04	RW	Frame Length High Byte
0x30B3	VTS_L	0x65	RW	Frame Length Low Byte
0x30B6	CEXP_DCG_H	0x00	RW	Frame DCG (HCG/LCG) Exposure Time (Coarse/in Rows) High Byte
0x30B7	CEXP_DCG_L	0x10	RW	Frame DCG (HCG/LCG) Exposure Time (Coarse/in Rows) Low Byte
0x30C9	EXP_DCG_H	–	R	Frame DCG (HCG/LCG) Exposure Time (in Rows) High Byte
0x30CA	EXP_DCG_L	–	R	Frame DCG (HCG/LCG) Exposure Time (in Rows) Low Byte

3.7 black level calibration (BLC)

The black level correction (BLC) function is used to set the pixel output of a complete black object to a programmable pedestal value in all kinds of lightning conditions. Due to circuit offset and pixel dark current, the pixel output level of a black object is normally non-zero. The OV2718 calibrates the black level of the active pixel by subtracting the true optical black pixel output.

The target BLC pedestal value for HCG and LCG channels are set by registers {0x3160, 0x3161}and {0x3162, 0x3163}, respectively. The pedestals are 12-bit values. The ISP will subtract the pedestal value early in the signal processing path.

When the BLC is enabled, the active pixel output value will be limited to 0xFFF after subtracting the optical black pixel value. The BLC value can be manually overridden enabled by the registers 0x3140[4] for HCG and 0x3140[5] for LCG. In this case, the BLC function is disabled.

3.7.1 advanced operation of the BLC

The BLC is based on measuring the value at the center of the distribution of the optical black reference pixels and applying digital correction to bring the center to the predefined target value. The center of the pixel distribution is estimated from a combination of median and average filtering. The filtering for the BLC is based on the middle 1024 columns of the 8 optical dark rows. Only the values closest to the horizontal center of each row are used in order to minimize influence from any edge effects in the array.

During normal operation, dark current is expected to change slowly with time. During slow changes, the BLC in the OV2718 will not change the correction value before a certain delta is measured. This triggering is configurable in the blc_trigger_threshold registers for HCG and LCG captures in registers 0x314F and 0x3150, respectively. When one of these thresholds is crossed, the correction value is updated with an exponential moving average smoothing filter. The fractional smoothing factor is configurable in 0x3141 and affects the α in:

$correction_{FILTER} = correction_{LAST} + \alpha \times (correction_{NEW} - correction_{LAST}), 0 \leq \alpha \leq 1$

α is encoded as a 5-bit register value, so that α = (smoothing+1)/32. Setting smoothing to 0 means that no update is applied, while setting smoothing to 31 means that the new value is directly applied without smoothing.

Triggering the BLC is done to avoid changing the BLC correction on every frame, possibly leading to unwanted flickering. When the BLC is in trigger-mode, it is disabled (dark-level is not updated) until a condition (trigger) happens. There are multiple sources of triggers for the BLC:

- restart frame triggering
- exposure changed triggering
- gain changed triggering
- threshold triggering
- manual triggering (register write)

When triggered, the BLC is updated in a number of frames determined by restart_frames register (0x3156). Two kinds of responses can be taken:

- Hard trigger, where the first frame is applied directly (no filtering), while restart_frames registers are run with filtering. If direct application is wanted for all restart_frames, set smoothing to maximum.
- Soft trigger, where blc_restart_frames are applied with filtering.

Restart frame, exposure or gain changed are always hard triggers. Threshold and manual triggers can be either hard or soft. There are two thresholds for each capture. The hard threshold will always cause a hard trigger while the main threshold can be programmed to be soft or hard like in previous sensors. A trigger will always cause BLC for all captures to be triggered.

Threshold triggering occurs when the absolute difference between current measured dark level and currently applied dark level is larger than a configurable amount. All three captures are monitored and can cause a threshold trigger.

If triggering is not enabled, the BLC will be operating in every frame. When using filter mode, triggers can still cause hard triggers.

After a trigger, it is possible to have the BLC soft-triggered for a number of frames, restart_frames register (0x3156). This can help average noise over multiple frames after a hard trigger.

It is possible to disable the threshold crossed triggers by writing the blc_trigger_threshold registers to 0xFF. It is also possible to handle the threshold crossed triggers as hard triggers by setting the 0x314E[1] bit to 1.

Manual triggering is possible by writing a 1 to the 0x314E[0] bit. Note that this bit must be manually cleared. To manually cause a hard-trigger, the 0x314E[1] bit must also be set.

The maximum correction value can be programmed by registers blc_max_correction (0x3158 and 0x3159).

table 3-6 BLC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3140	BLC_CTRL	0x02	RW	Bit[7:4]: Not used Bit[3]: blc_cont_update_mode Enable BLC recalculation on every frame Bit[2]: Not used Bit[1]: blc_dither_en Enable dithering on unused sub-LSBS of incoming data Bit[0]: show_dark_rows Show the dark rows in the image
0x3141	BLC_SMOOTHING	0x07	RW	Filter Coefficient Alpha = (Smoothing+1)/32. If Zero, New Value Is Not Used.
0x3142	D_VALUE_HCG	0x00	RW	Signed Fractional (/256) Value Between -128/256 and 128/256 to Adjust DL'=DL(1+D) for HCG Exposure

table 3-6 BLC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3143	D_VALUE_LCG	0x00	RW	Signed Fractional (/256) Value Between -128/256 and 128/256 to Adjust DL'=DL(1+D) for LCG Exposure
0x3145	K_OFFSET_HCG	0x00	RW	Signed Offset to Adjust DL' = DL + K × again/16 for HCG Exposure
0x3146	K_OFFSET_LCG	0x00	RW	Signed Offset to Adjust DL' = DL + K × again/16 for LCG Exposure
0x3148	BLC_OVERRIDE_HCG_H	0x00	RW	Manual BLC Override Value for HCG Exposure MSB
0x3149	BLC_OVERRIDE_HCG_L	0x00	RW	Manual BLC Override Value for HCG Exposure LSB
0x314A	BLC_OVERRIDE_LCG_H	0x00	RW	Manual BLC Override Value for LCG Exposure MSB
0x314B	BLC_OVERRIDE_LCG_L	0x00	RW	Manual BLC Override Value for LCG Exposure LSB
0x314E	BLC_TRIGGER	0x1C	RW	Bit[7:5]: Not used Bit[4]: blc_exp_changed_trig_en Enable triggering of BLC after exposure changes Bit[3]: blc_gain_changed_trig_en Enable triggering of BLC after gain changes Bit[2]: blc_restart_frame_trig_en Enable triggering of BLC at restart Bit[1]: blc_hard_trigger_en Enable hard triggering for manual, threshold crossed, and continuos update triggers as well Bit[0]: blc_manual_trig Transition 0->1 causes trigger. Must be reset by user.
0x314F	BLC_TRIGGER_THRE_HCG	0x10	RW	Threshold for Triggering of BLC for HCG Exposure (no sub-LSBS). 0xFF Will Turn Threshold Triggering Off. The Difference Between Dark Level for Current Frame and Applied Correction Is Compared to the Threshold.
0x3150	BLC_TRIGGER_THRE_LCG	0x10	RW	Threshold for Triggering of BLC for LCG Exposure (no sub-LSBS). 0xFF Will Turn Threshold Triggering Off. The Difference Between Dark Level for Current Frame and Applied Correction Is Compared to the Threshold.

table 3-6 BLC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3152	BLC_TRIGGER_THRE_HARD_HCG	0x80	RW	Threshold for Hard Triggering of BLC for HCG Exposure (no sub-LSBS). 0xFF Will Turn Hard Threshold Triggering Off. The Difference Between Dark Level for Current Frame and Applied Correction Is Compared to the Threshold.
0x3153	BLC_TRIGGER_THRE_HARD_LCG	0x80	RW	Threshold for Hard Triggering of BLC for LCG Exposure (no sub-LSBS). 0xFF Will Turn Hard Threshold Triggering Off. The Difference Between Dark Level for Current Frame and Applied Correction Is Compared to the Threshold.
0x3155	DITHER_GAIN_THRESHOLD	0x00	RW	Gain Threshold for Enabling Dither. Compared to Upper 8 Bits of Digital Gain Value. A Value of 0 Means Always Enabled.
0x3156	RESTART_FRAMES	0x01	RW	Number of Frames With Continuous Update After Restart. 0xFF Is Always Triggered, 0x00 Will Give 1 Frame.
0x3157	AB_CTRL	0x00	RW	Controls AB Mode Operation Bit[7:2]: Not used Bit[1]: Bframe Selects between A (0) and B (1) frames Bit[0]: ab_mode Enable AB mode
0x3158	BLC_MAX_CORRECTION_H	0x0F	RW	Maximum Value of BLC Correction MSB
0x3159	BLC_MAX_CORRECTION_L	0xFF	RW	Maximum Value of BLC Correction LSB
0x315A	DIG_GAIN_HCG_H	0x01	RW	Digital Gain for HCG MSB (Format 6.8)
0x315B	DIG_GAIN_HCG_L	0x00	RW	Digital Gain for HCG LSB
0x315C	DIG_GAIN_LCG_H	0x01	RW	Digital Gain for LCG MSB (Format 6.8)
0x315D	DIG_GAIN_LCG_L	0x00	RW	Digital Gain for LCG LSB
0x3160	BLC_TARGET_HCG_H	0x00	RW	Black Level Target HCG Exposure High Byte
0x3161	BLC_TARGET_HCG_L	0x20	RW	Black Level Target HCG Exposure Low Byte
0x3162	BLC_TARGET_LCG_H	0x00	RW	Black Level Target LCG Exposure High Byte
0x3163	BLC_TARGET_LCG_L	0x20	RW	Black Level Target LCG Exposure Low Byte
0x3166	DIG_GAIN_FS2_HCG_H	–	R	Read Back of Frame Synchronized Digital Gain for HCG Exposure MSB

table 3-6 BLC control registers (sheet 4 of 4)

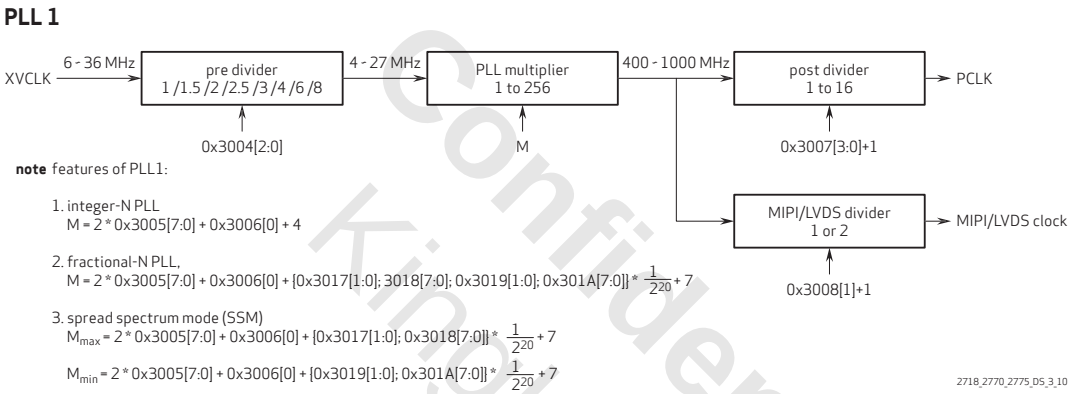
address	register name	default value	R/W	description
0x3167	DIG_GAIN_FS2_HCG_L	–	R	Read Back of Frame Synchronized Digital Gain for HCG Exposure LSB
0x3168	DIG_GAIN_FS2_LCG_H	–	R	Read Back of Frame Synchronized Digital Gain for LCG Exposure MSB
0x3169	DIG_GAIN_FS2_LCG_L	–	R	Read Back of Frame Synchronized Digital Gain for LCG Exposure LSB
0x316A	DIG_GAIN_FS2_HCG_H	–	R	Read Back of Frame Synchronized Digital Gain for HCG Exposure MSB

3.8 PLL

PLL settings can only be changed during sensor standby mode (0x3012 = 0).

The OV2718 implements two PLLs with both inputs connected to the XVCLK pin. One can support the MIPI/LVDS bit clock and output clock PCLK, while the other one can support internal SCLK. Two PLLs enable the internal clock (SCLK) to be separate from the output clock (PCLK). Additionally, the two PLLs, in MIPI/LVDS mode, can be used to optimize for EMC and/or minimize the required MIPI frequency.

figure 3-9 PLL1 control diagram



In order to reduce EMI's impact, this PLL also supports spread spectrum mode (SSM). Spread profile is a triangular waveform spread. The spectrum can be up spread, both side spread, or down spread depend on the input setting dsm[19:0]. Tssc is the modulation period. Fssc(1/Tssc) is the modulation frequency, which is about 30KHz~33KHz in many interface design. DeltaF is modulation amplitude, which is normally smaller than 5000ppm. For example, if normal clock frequency Fo=1GHz, then 5000ppm=5000×Fo/1e6=5MHz.

$$Fmax = \frac{RefClk}{PreDiv} \cdot [2 * pdiv[7:0] + 7 + sdiv + dsm[19:10] \cdot (\frac{1}{2^9})]$$

$$Fmin = \frac{RefClk}{PreDiv} \cdot [2 * pdiv[7:0] + 7 + sdiv + dsm[9:0] \cdot (\frac{1}{2^9})]$$

figure 3-10 PLL2 control diagram

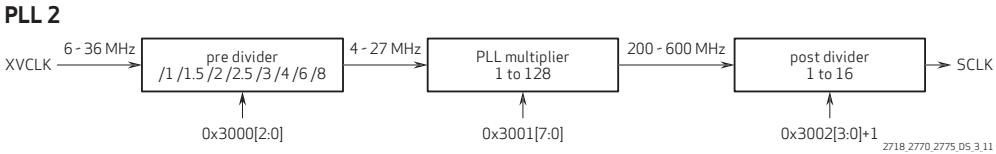


table 3-7 PLL control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3000	SCLK_PLL_PRE	0x05	RW	SCLK PLL Pre Divider
0x3001	SCLK_PLL_MULT	0x63	RW	SCLK PLL Multiplier
0x3002	SCLK_PLL_POST	0x03	RW	SCLK PLL Post Divider (1~16)
0x3003	SCLK_PLL_CONFIG	0x01	RW	Bit[7:6]: lock_precision Lock detector precision resolution setting Bit[5:4]: lock_cntref Lock detector counter setting Bit[3]: fastlock_disable 0: Enable fast locking 1: Disable fast locking Bit[2:0]: Cp Charge pump current
0x3004	PCLK_PLL_PRE	0x06	RW	PCLK PLL Pre Divider
0x3005	PCLK_PLL_PDIV	0x7B	RW	PCLK PLL Div 1 (1~256)
0x3006	PCLK_PLL_SDIV	0x00	RW	PCLK PLL Div 2
0x3007	PCLK_PLL_POST	0x07	RW	PCLK PLL Post Divider (1~16)
0x3008	PCLK_PLL_CTRL1	0x01	RW	Bit[7:2]: Not used Bit[1]: pclk_pll_mipi_div Divide frequency to MIPI/LVDS by 2 Bit[0]: pclk_pll_enable Enable PLL1
0x3009	PCLK_PLL_CTRL2	0x00	RW	Bit[7]: Not used Bit[6:5]: ssc_cntstep Select SSC counter step number Bit[4:2]: ssc_cntck Set SSC counter frequency Bit[1]: ssc_en Enable SSC mode Bit[0]: frac_en Enable fractional mode
0x3017	PCLK_PLL_DSM_MAX_H	0x00	RW	PCLK PLL Fractional Div[19:18] (SSC Maximum High Byte)
0x3018	PCLK_PLL_DSM_MAX_L	0x00	RW	PCLK PLL Fractional Div[17:10] (SSC Maximum Low Byte)
0x3019	PCLK_PLL_DSM_MIN_H	0x00	RW	PCLK PLL Fractional Div[9:8] (SSC Minimum High Byte)

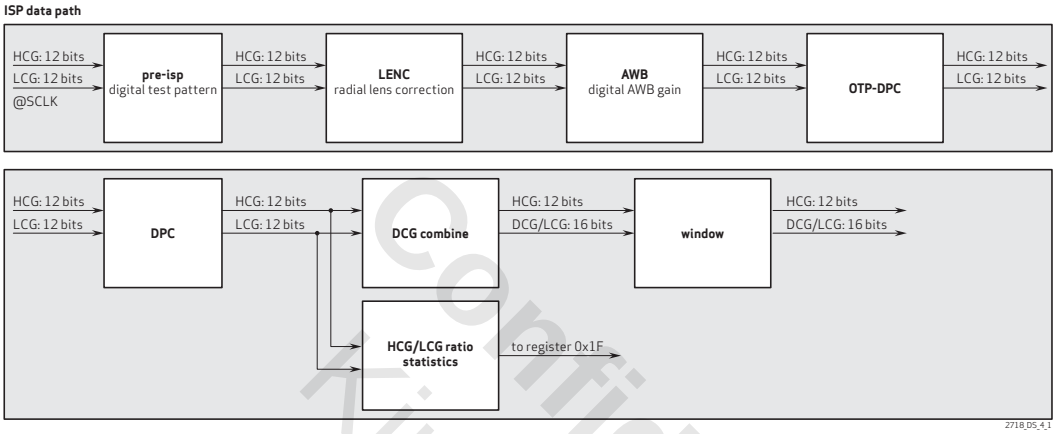
table 3-7 PLL control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x301A	PCLK_PLL_DSM_MIN_L	0x00	RW	PCLK PLL Fractional Div[7:0] (SSC Minimum Low Byte)
0x301B	PCLK_PLL_CONFIG	0x01	RW	Bit[7:6]: lock_precision Lock detector precision resolution setting Bit[5:4]: lock_cntref Lock detector counter setting Bit[3]: fastlock_disable 0: Enable fast locking 1: Disable fast locking Bit[2:0]: Cp Charge pump current

4 image processor

figure 4-1 shows the top level block diagram of the OV2718 image processor.

figure 4-1 image processor block diagram



The ISP receives image data from the sensor core and includes modules for RAW image processing. The video stream arrives as 12-bit parallel data separated in high conversion gain (HCG), low conversion gain (LCG) capture channels. Unused rows and columns are cut before further processing. After processing the data from the ISP, it is configured to the correct output format in the output interface.

One of the first processing steps in the ISP is to correct the shading caused by lens fall off (LENC). Digital gain is then applied to make the image white balanced (AWB gain). Defect pixel and clusters (DPC) are corrected on-the-fly for each captures. After that the DCG exposures (HCG and LCG) are combined into a 16-bit HDR image (DCG combine). In the transition area, the data is linearly combined.

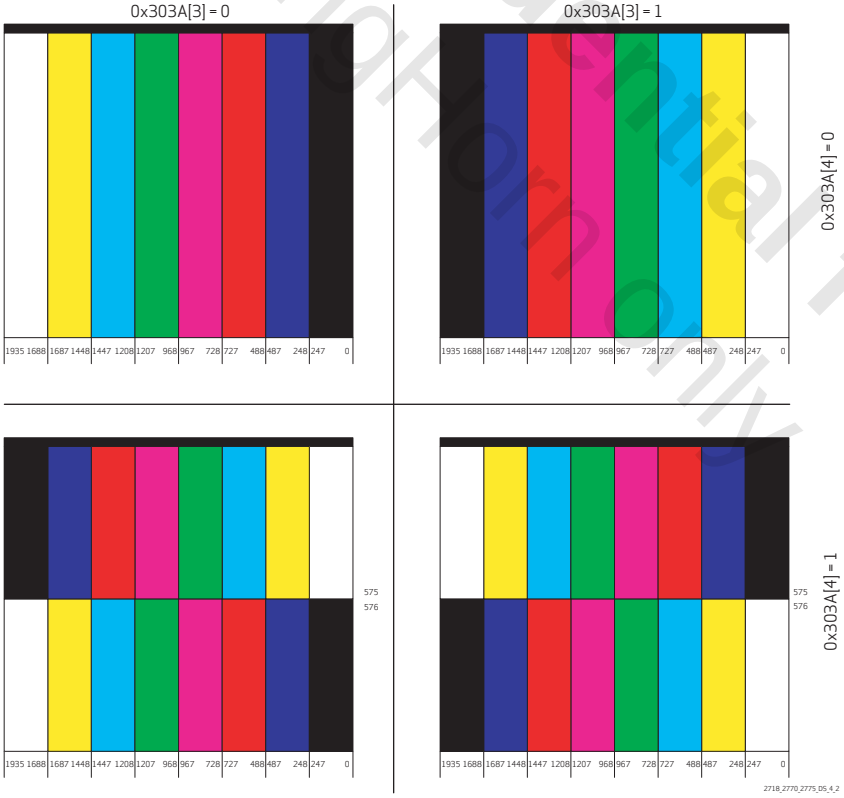
4.1 test pattern

For testing purposes, the OV2718 offers analog and digital test patterns. The analog test pattern is a color bar as an overlay image (test pattern applied on pixel output to exercise the whole analog readout channel) and is enabled by setting register 0x303A[5] = 1. The intensity of this color bar can be controlled by register 0x303A[2:0] and the order of colors can be swapped by setting register 0x303A[3] = 1. The OV2718 also offers two digital effects for the test patterns: transparent effect and rolling bar effect. The digital test pattern function is enabled by register 0x3253[7] and the test pattern is selected by register 0x3253[6:0]. The test patterns are only available if the ISP is enabled (0x3250[0] = 1). The test patterns are processed by the ISP and outputted as regular images. However, they are unaffected by sensor exposure time and digital gain.

4.1.1 analog color bar overlay

The analog color bar overlay is enabled by setting register 0x303A[5] = 1, the overlay patterns are selected by programming 0x303A[4:3] (see **figure 4-2**) and the color intensity is adjusted by programming register 0x305A[2:0]. **figure 4-2** also shows how the color bar patterns are mapped to the physical row and column addresses. The location of the mid-array rows, where the patterns are swapped, as well as the color bar borders, remain the same regardless if the image is cropped or not.

figure 4-2 color bar types



4.1.2 digital test patterns

The data path test patterns are only available if the ISP is enabled (0x3250[0] = 1). The test patterns are processed by the ISP and outputted as regular images. However, they are unaffected by sensor exposure time and digital gain.

figure 4-3 vertical bars test pattern

figure 4-4 vertical bars with vertical gradient test pattern

figure 4-5 vertical bars with horizontal gradient test pattern

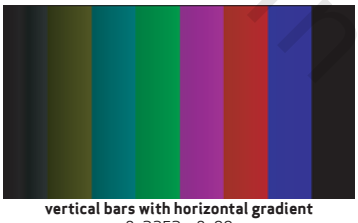


figure 4-6 vertical bars with diagonal gradient test pattern

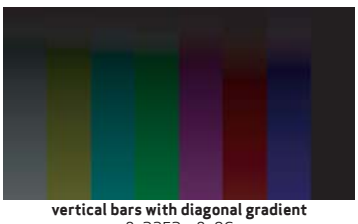
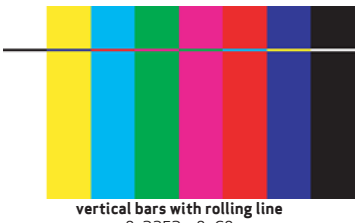


figure 4-7 vertical bars with rolling line test pattern

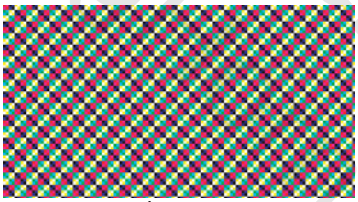


vertical bars with rolling line
0x3253 = 0xC0 2718_2770_2775_DS_4.7

figure 4-8 random image test pattern

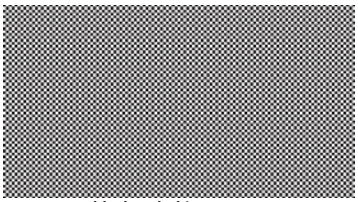
random image
0x3253 = 0x81 2718_2770_2775_DS_4.8

figure 4-9 color squares test pattern



color squares
0x3253 = 0x82 2718_2770_2775_DS_4.9

figure 4-10 black and white squares test pattern



black and white squares
0x3253 = 0x92 2718_2770_2775_DS_4.10

figure 4-11 chart test pattern

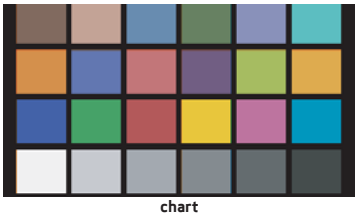


table 4-1 test pattern control registers

address	register name	default value	R/W	description
0x303A	ANA_CB	0x04	RW	Bit[7:6]: Not used Bit[5]: cb_en Enable color bars Bit[4]: cb_mode 0: Do not swap color bars mid-array 1: Swap color bars mid-array (mirror rows) Bit[3]: cb_swap 0: Do not swap color bars 1: Swap color bars (mirror columns) Bit[2:0]: cb_adjust LCB current level (color bar intensity)
0x3250	ISP_DP_CONF1	0x33	RW	Bit[7]: dpc_bc_en Black pixel correction enable in DPC Bit[6]: dpc_wc_en White pixel correction enable in DPC Bit[5]: isp_out_window_en (active high, default high) ISP output window crop enable Bit[4]: Not used Bit[3]: lenc_en Enable lens correction Bit[2]: otp_en Defect pixel tagging enable Bit[1]: awb_gain_en AWB_gain enable Bit[0]: isp_en (active high, default high) ISP enable

4.2 lens correction (LENC)

The first step in the image processing pipeline is to correct the shading due to light fall off in the edges and corner areas. The correction is done by multiplying each pixel with a gain based on the area where each pixel is located. The control points are separated for red, green and blue (see registers 0x3330~0x3347). LENC is disabled by default and can be enabled by register 0x3250[3]. LENC is not supported in linear mode.

The OV2718 supports sub-sampling and flip in both horizontal and vertical directions while LENC is enabled.

The LENC control registers are separate for red, green and blue.

Under dark conditions, the signal-to-noise ratio (SNR) drops in the corner areas. The noise can be significantly amplified by the lens correction gain and results in a brighter corner. The OV2718 can automatically adjust gain for the pixels to adapt to lighting conditions. This is accomplished by following the sensor analog gain and is enabled through register 0x3348[2].

LENC uses the following formula to generate the gain:

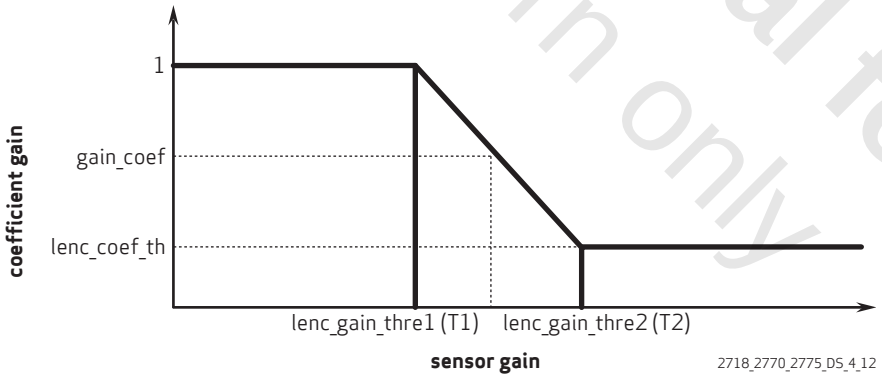
gain=a*r*r+b*r+1

where a and b is set by registers 0x3334~0x3337 for red, registers 0x333C~0x333F for green, and registers 0x3344~0x3347 for blue. R is the distance to the center of the image (center of the lens), that is, radius. "Gain" for center pixel is 1 (the minimum). "Gain" for perimeter pixels has a maximum of 5.

The parameters a and b also can be adjusted by the sensor gain.

The relationship of calculating the coefficient gain is shown in **figure 4-12**.

figure 4-12 coefficient gain graph



LENC control point parameters must be calibrated with a specific tool. Please contact your regional OmniVision FAE for assistance.

table 4-2 LENC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x30A0	CROP_H_ST_H	0x00	RW	Start Address Horizontal High Byte
0x30A1	CROP_H_ST_L	0x00	RW	Start Address Horizontal Low Byte
0x30A2	CROP_V_ST_H	0x00	RW	Start Address Vertical High Byte
0x30A3	CROP_V_ST_L	0x00	RW	Start Address Vertical Low Byte
0x30A4	CROP_H_END_H	0x07	RW	End Address Horizontal High Byte
0x30A5	CROP_H_END_L	0x8F	RW	End Address Horizontal Low Byte
0x30A6	CROP_V_END_H	0x04	RW	End Address Vertical High Byte
0x30A7	CROP_V_END_L	0x47	RW	End Address Vertical Low Byte
0x3250	ISP_DP_CONF1	0x33	RW	Bit[3]: lenc_en Enable lens correction
0x3330	LENC_RED_X0_H	0x03	RW	Red Center Horizontal Position (X0) High Byte
0x3331	LENC_RED_X0_L	0xC8	RW	Red Center Horizontal Position (X0) Low Byte
0x3332	LENC_RED_Y0_H	0x02	RW	Red Center Vertical Position (Y0) High Byte
0x3333	LENC_RED_Y0_L	0x24	RW	Red Center Vertical Position (Y0) Low Byte
0x3334	LENC_RED_A1	0x00	RW	Red Parameter A1
0x3335	LENC_RED_A2	0x00	RW	Red Parameter A2
0x3336	LENC_RED_B1	0x00	RW	Red Parameter B1
0x3337	LENC_RED_B2	0x00	RW	Red Parameter B2
0x3338	LENC_GRN_X0_H	0x03	RW	Green Center Horizontal Position (X0) High Byte
0x3339	LENC_GRN_X0_L	0xC8	RW	Green Center Horizontal Position (X0) Low Byte
0x333A	LENC_GRN_Y0_H	0x02	RW	Green Center Vertical Position (Y0) High Byte
0x333B	LENC_GRN_Y0_L	0x24	RW	Green Center Vertical Position (Y0) Low Byte
0x333C	LENC_GRN_A1	0x00	RW	Green Parameter A1
0x333D	LENC_GRN_A2	0x00	RW	Green Parameter A2
0x333E	LENC_GRN_B1	0x00	RW	Green Parameter B1
0x333F	LENC_GRN_B2	0x00	RW	Green Parameter B2
0x3340	LENC_BLU_X0_H	0x03	RW	Blue Center Horizontal Position (X0) High Byte
0x3341	LENC_BLU_X0_L	0xC8	RW	Blue Center Horizontal Position (X0) Low Byte

table 4-2 LENC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3342	LENC_BLU_Y0_H	0x02	RW	Blue Center Vertical Position (Y0) High Byte
0x3343	LENC_BLU_Y0_L	0x24	RW	Blue Center Vertical Position (Y0) Low Byte
0x3344	LENC_BLU_A1	0x00	RW	Blue Parameter A1
0x3345	LENC_BLU_A2	0x00	RW	Blue Parameter A2
0x3346	LENC_BLU_B1	0x00	RW	Blue Parameter B1
0x3347	LENC_BLU_B2	0x00	RW	Blue Parameter B2
0x3348	LENC_CTRL	0x40	RW	Bit[7]: Not used Bit[6]: lenc_bias_plus Add bias back after LENC Bit[5:4]: real_gain_sel Select real gain to use for coefficient adjustment 00: HGC 01: LCG 10: Not used 11: Not used Bit[3]: coef_man_en Override LENC gain coefficient with lenc_coef_man Bit[2]: gcoef_en Enables gain coefficient adjustment Bit[1]: quad_acc_en Bit[0]: rnd_en Adds random bits
0x3349	LENC_COEF_THRE	0x00	RW	Coefficient Threshold (Minimum Level of Coefficient Gain) Format: 1.7, Max: 1.0
0x334A	LENC_GAIN_THRE1_H	0x00	RW	ISP Real Gain Threshold Low (No Sub-LSB) High Byte
0x334B	LENC_GAIN_THRE1_L	0x00	RW	ISP Real Gain Threshold Low (No Sub-LSB) Low Byte
0x334C	LENC_GAIN_THRE2_H	0x00	RW	ISP Real Gain Threshold High (No Sub-LSB) High Byte
0x334D	LENC_GAIN_THRE2_L	0x00	RW	ISP Real Gain Threshold High (No Sub-LSB) Low Byte
0x334E	LENC_COEF_MAN	0x80	RW	Manual Coefficient Scaling Parameter Format: 1.7, Max: 1.0

4.3 auto white balance gain (AWB gain)

The next process in the pipeline is white balance. The RAW red, green and blue values of a gray object vary with the light source spectrum and the pixel QE spectrum response. Light source spectrum is usually described by "color temperature", which is the surface temperature of a black body radiating equivalent spectrum. In the real world, the light color temperature ranges from very low (reddish) to very high (bluish) value. For example, the color temperature of an incandescent lamp is about 2850K, while the color temperature of an overcast day is about 6500K.

To make sure that a gray image is truly gray regardless of the light spectrum, the sensor needs to adjust the gain for each RGB channel according to color temperature. This process is called white balance (WB).

The OV2718 WB gain registers can be controlled by a separate ISP processor.

The offset must be set by the registers 0x3378~0x338F for each capture channel and color channel. The offset value is calculated as:

offset = (AWB_gain - 1) × blc_target

White balance gain is enabled/disabled in register 0x3250[1]. The applied WB gain can be read back from registers 0x3360~0x336F and offset values can be read back from registers 0x3378~0x338F.

table 4-3 AWB control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3250	ISP_DP_CONF1	0x33	RW	Bit[1]: awb_gain_en AWB_gain enable
0x3360	R_GAIN_HCG_H	0x01	RW	Gain High Bits for HCG Channel Red Component
0x3361	R_GAIN_HCG_L	0x00	RW	Gain Low Bits for HCG Channel Red Component
0x3362	GR_GAIN_HCG_H	0x01	RW	Gain High Bits for HCG Channel Greenr Component
0x3363	GR_GAIN_HCG_L	0x00	RW	Gain Low Bits for HCG Channel Greenr Component
0x3364	GB_GAIN_HCG_H	0x01	RW	Gain High Bits for HCG Channel Greenb Component
0x3365	GB_GAIN_HCG_L	0x00	RW	Gain Low Bits for HCG Channel Greenb Component
0x3366	B_GAIN_HCG_H	0x01	RW	Gain High Bits for HCG Channel Blue Component
0x3367	B_GAIN_HCG_L	0x00	RW	Gain Low Bits for HCG Channel Blue Component
0x3368	R_GAIN_LCG_H	0x01	RW	Gain High Bits for LCG Channel Red Component
0x3369	R_GAIN_LCG_L	0x00	RW	Gain Low Bits for LCG Channel Red Component

table 4-3 AWB control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x336A	GR_GAIN_LCG_H	0x01	RW	Gain High Bits for LCG Channel Greenr Component
0x336B	GR_GAIN_LCG_L	0x00	RW	Gain Low Bits for LCG Channel Greenr Component
0x336C	GB_GAIN_LCG_H	0x01	RW	Gain High Bits for LCG Channel Greenb Component
0x336D	GB_GAIN_LCG_L	0x00	RW	Gain Low Bits for LCG Channel Greenb Component
0x336E	B_GAIN_LCG_H	0x01	RW	Gain High Bits for LCG Channel Blue Component
0x336F	B_GAIN_LCG_L	0x00	RW	Gain Low Bits for LCG Channel Blue Component
0x3378	R_OFFSET_HCG_H	0x00	RW	Offset High Bits for HCG Channel Red Component
0x3379	R_OFFSET_HCG_M	0x00	RW	Offset Medium Bits for HCG Channel Red Component
0x337A	R_OFFSET_HCG_L	0x00	RW	Offset Low Bits for HCG Channel Red Component
0x337B	GR_OFFSET_HCG_H	0x00	RW	Offset High Bits for HCG Channel Greenr Component
0x337C	GR_OFFSET_HCG_M	0x00	RW	Offset Medium Bits for HCG Channel Greenr Component
0x337D	GR_OFFSET_HCG_L	0x00	RW	Offset Low Bits for HCG Channel Greenr Component
0x337E	GB_OFFSET_HCG_H	0x00	RW	Offset High Bits for HCG Channel Greenb Component
0x337F	GB_OFFSET_HCG_M	0x00	RW	Offset Medium Bits for HCG Channel Greenb Component
0x3380	GB_OFFSET_HCG_L	0x00	RW	Offset Low Bits for HCG Channel Greenb Component
0x3381	B_OFFSET_HCG_H	0x00	RW	Offset High Bits for HCG Channel Blue Component
0x3382	B_OFFSET_HCG_M	0x00	RW	Offset Medium Bits for HCG Channel Blue Component
0x3383	B_OFFSET_HCG_L	0x00	RW	Offset Low Bits for HCG Channel Blue Component
0x3384	R_OFFSET_LCG_H	0x00	RW	Offset High Bits for LCG Channel Red Component

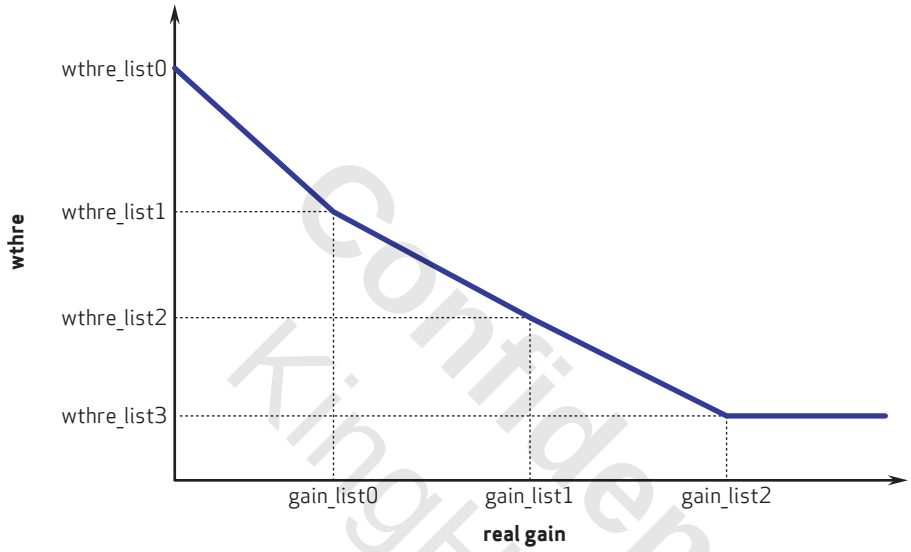
table 4-3 AWB control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3385	R_OFFSET_LCG_M	0x00	RW	Offset Medium Bits for LCG Channel Red Component
0x3386	R_OFFSET_LCG_L	0x00	RW	Offset Low Bits for LCG Channel Red Component
0x3387	GR_OFFSET_LCG_H	0x00	RW	Offset High Bits for LCG Channel Greenr Component
0x3388	GR_OFFSET_LCG_M	0x00	RW	Offset Medium Bits for LCG Channel Greenr Component
0x3389	GR_OFFSET_LCG_L	0x00	RW	Offset Low Bits for LCG Channel Greenr Component
0x338A	GB_OFFSET_LCG_H	0x00	RW	Offset High Bits for LCG Channel Greenb Component
0x338B	GB_OFFSET_LCG_M	0x00	RW	Offset Medium Bits for LCG Channel Greenb Component
0x338C	GB_OFFSET_LCG_L	0x00	RW	Offset Low Bits for LCG Channel Greenb Component
0x338D	B_OFFSET_LCG_H	0x00	RW	Offset High Bits for LCG Channel Blue Component
0x338E	B_OFFSET_LCG_M	0x00	RW	Offset Medium Bits for LCG Channel Blue Component
0x338F	B_OFFSET_LCG_L	0x00	RW	Offset Low Bits for LCG Channel Blue Component

4.4 defective pixel cancellation (DPC)

The DPC function detects defect pixels/clusters by using a programmable threshold. The threshold can be set manually by registers or automatically calculated based on analog gain. Refer to figure **figure 4-13** for details.

figure 4-13 threshold gain curve

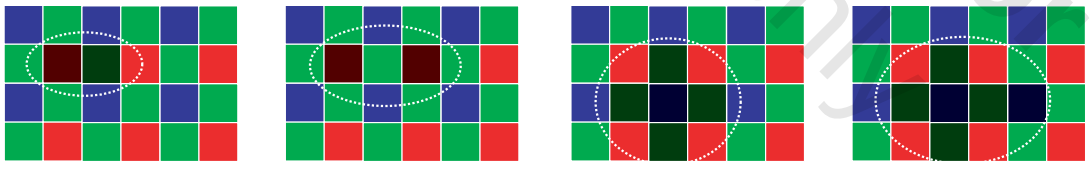


note Bthre = Wthre * (8+thre_ratio)/8

2718_2770_2775_DS_4_13

The DPC can correct single defect pixel, couplet, cross type and tail type cluster (refer to **table 4-4** for the enable/disable controls for each type of defect). **figure 4-14** shows the sample defect pattern of couplet, cross and tail cluster defect.

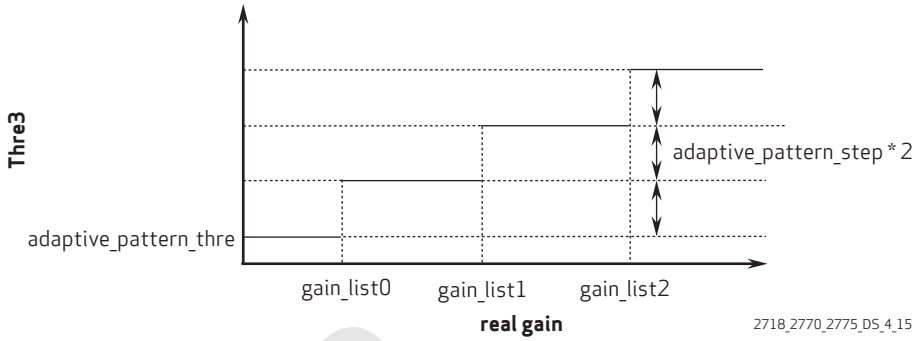
figure 4-14 defect pattern examples



different color plane couplet | same color plane couplet | cross type cluster | tail type cluster

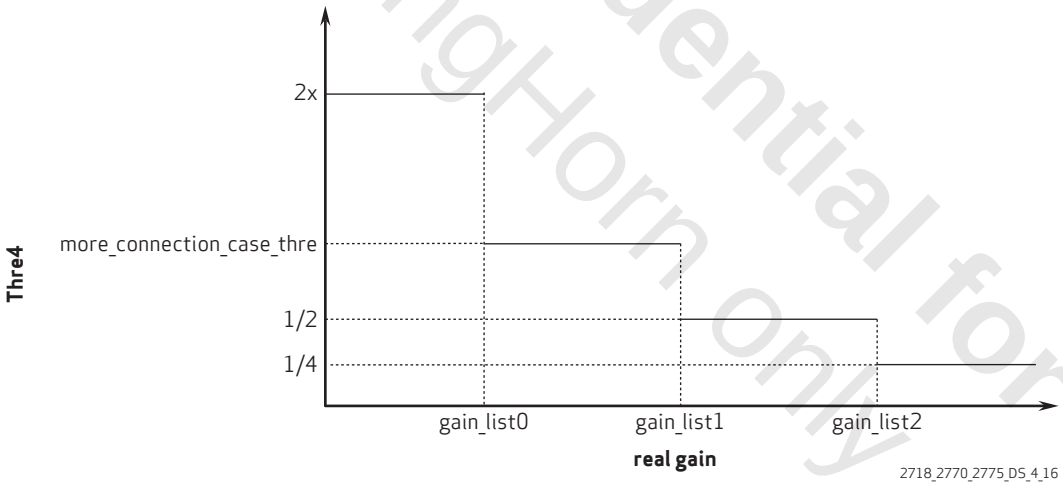
2718_2770_2775_DS_4_14

figure 4-15 adaptive thresholds



If there are two similar defective pixels not far from each other, they cannot be recovered. To resolve this, the DPC algorithm will only search for similar patterns in high frequency regions. When the difference between minimum and maximum values are below the adaptive threshold, the current pixel is considered located in a high frequency region. Smaller threshold values will retain more image details.

figure 4-16 connected case thresholds



When detecting the same or different channel connected defect pixels, the difference between the central pixel and surrounding normal pixels must be below this threshold. Compared to a single white or black pixel, these clusters will further degrade the image quality, thus a separate threshold is designed for them. These thresholds are higher than single defect pixel thresholds as connected cases are less common.

table 4-4 DPC registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x33F5	CTRL_DPC_00_HCG	0x14	RW	Bit[7:6]: Not used Bit[5]: Tail enable Crosscluster must also be enabled Bit[4]: Saturate crosscluster enable Crosscluster must also be enabled Bit[3]: 3x3 cluster enable Bit[2]: Crosscluster enable Bit[1]: General tail enable Three horizontal connected clusters with one of the pixels exceeding the saturation value Bit[0]: Manual mode enable
0x33F6	CTRL_DPC_01_HCG	0x0F	RW	Bit[7:4]: Saturate pixel saturation threshold Bit[3]: Different channel white pixel correction enable Bit[2]: Different channel black pixel correction enable Bit[1]: Same channel white pixel correction enable Bit[0]: Same channel black pixel correction enable
0x33F7	CTRL_DPC_02_HCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list0 Threshold value for white pixel detection in manual mode
0x33F8	CTRL_DPC_03_HCG	0x02	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list1 Threshold value for white pixel detection in manual mode
0x33F9	CTRL_DPC_04_HCG	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list2 Threshold value for white pixel detection in manual mode
0x33FA	CTRL_DPC_05_HCG	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list3 Threshold value for white pixel detection in manual mode
0x33FB	CTRL_DPC_06_HCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern thresholds
0x33FC	CTRL_DPC_07_HCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern step
0x33FD	CTRL_DPC_08_HCG	0x0C	RW	Bit[7:4]: Not used Bit[3:0]: More connection case thresholds

table 4-4 DPC registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x33FE	CTRL_DPC_09_HCG	0x00	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list0 DPC level is used to remove different types of clusters. Higher levels mean more defective clusters removed, but image quality will worsen
0x33FF	CTRL_DPC_10_HCG	0x01	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list1
0x3400	CTRL_DPC_11_HCG	0x02	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list2
0x3401	CTRL_DPC_12_HCG	0x03	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list3
0x3402	CTRL_DPC_13_HCG	0x03	RW	Bit[7]: Not used Bit[6:0]: Gain list0
0x3403	CTRL_DPC_14_HCG	0x0F	RW	Bit[7]: Not used Bit[6:0]: Gain list1
0x3404	CTRL_DPC_15_HCG	0x3F	RW	Bit[7]: Not used Bit[6:0]: Gain list2
0x3405	CTRL_DPC_16_HCG	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Matching thresholds If a similar pattern in the neighbor of the central defect pixel is found, this value will be used to replace the current defect pixel. This threshold is used to determine similarity between pixels. If the difference between two pixels is larger than this threshold, the two are not considered similar. Larger threshold will maintain more image detail.
0x3406	CTRL_DPC_17_HCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Status thresholds A pixel is marked as defective if the original and recovered value is larger than this threshold. More defective pixels will be removed with a larger threshold while removing image details.
0x3407	CTRL_DPC_18_HCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: wb_th_ratio Ratio of white threshold and black threshold

table 4-4 DPC registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x3408	CTRL_DPC_19_HCG	0x00	RW	Bit[7:1]: Not used Bit[0]: Clip interpolate G enable Controls whether or not to remove defective pixels in the B or R channel when G channel is saturated 0: Disable 1: Enable
0x3409	CTRL_DPC_20_HCG	0x03	RW	Bit[7:2]: Not used Bit[1:0]: edge_opt Image boundary process option 00: Pad zero to remove white pixels 01: Pad max value to remove black pixels 10: Duplicate the adjacent same channel data for padding 11: Duplicate the upper same channel data for padding
0x340A	CTRL_DPC_00_LCG	0x14	RW	Bit[7:6]: Not used Bit[5]: Tail enable Crosscluster must also be enabled Bit[4]: Saturate crosscluster enable Crosscluster must also be enabled Bit[3]: 3x3 cluster enable Bit[2]: Crosscluster enable Bit[1]: General tail enable Three horizontal connected clusters with one of the pixels exceeding the saturation value Bit[0]: Manual mode enable
0x340B	CTRL_DPC_01_LCG	0x0F	RW	Bit[7:4]: Saturate pixel saturation threshold Bit[3]: Different channel white pixel correction enable Bit[2]: Different channel black pixel correction enable Bit[1]: Same channel white pixel correction enable Bit[0]: Same channel black pixel correction enable
0x340C	CTRL_DPC_02_LCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list0 Threshold value for white pixel detection in manual mode
0x340D	CTRL_DPC_03_LCG	0x02	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list1 Threshold value for white pixel detection in manual mode

table 4-4 DPC registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x340E	CTRL_DPC_04_LCG	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list2 Threshold value for white pixel detection in manual mode
0x340F	CTRL_DPC_05_LCG	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list3 Threshold value for white pixel detection in manual mode
0x3410	CTRL_DPC_06_LCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern thresholds
0x3411	CTRL_DPC_07_LCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern step
0x3412	CTRL_DPC_08_LCG	0x0C	RW	Bit[7:4]: Not used Bit[3:0]: More connection case thresholds
0x3413	CTRL_DPC_09_LCG	0x00	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list0 DPC level is used to remove different types of clusters. Higher levels mean more defective clusters removed, but image quality will worsen
0x3414	CTRL_DPC_10_LCG	0x01	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list1
0x3415	CTRL_DPC_11_LCG	0x02	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list2
0x3416	CTRL_DPC_12_LCG	0x03	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list3
0x3417	CTRL_DPC_13_LCG	0x03	RW	Bit[7]: Not used Bit[6:0]: Gain list0
0x3418	CTRL_DPC_14_LCG	0x0F	RW	Bit[7]: Not used Bit[6:0]: Gain list1
0x3419	CTRL_DPC_15_LCG	0x3F	RW	Bit[7]: Not used Bit[6:0]: Gain list2

table 4-4 DPC registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x341A	CTRL_DPC_16_LCG	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Matching thresholds If a similar pattern in the neighbor of the central defect pixel is found, this value will be used to replace the current defect pixel. This threshold is used to determine similarity between pixels. If the difference between two pixels is larger than this threshold, the two are not considered similar. Larger threshold will maintain more image detail.
0x341B	CTRL_DPC_17_LCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Status thresholds A pixel is marked as defective if the original and recovered value is larger than this threshold. More defective pixels will be removed with a larger threshold while removing image details.
0x341C	CTRL_DPC_18_LCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: wb_th_ratio Ratio of white threshold and black threshold
0x341D	CTRL_DPC_19_LCG	0x00	RW	Bit[7:1]: Not used Bit[0]: Clip interpolate G enable Controls whether or not to remove defective pixels in the B or R channel when G channel is saturated 0: Disable 1: Enable
0x341E	CTRL_DPC_20_LCG	0x03	RW	Bit[7:2]: Not used Bit[1:0]: edge_opt Image boundary process option 00: Pad zero to remove white pixels 01: Pad max value to remove black pixels 10: Duplicate the adjacent same channel data for padding 11: Duplicate the upper same channel data for padding
0x3426	CTRL_DPC_21_HCG	–	R	Bit[7]: Not used Bit[6:0]: Black thresholds
0x3427	CTRL_DPC_22_HCG	–	R	Bit[7:5]: Not used Bit[4:0]: White thresholds
0x3428	CTRL_DPC_23_HCG	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 1

table 4-4 DPC registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x3429	CTRL_DPC_24_HCG	–	R	Bit[7:6]: Not used Bit[5:0]: Threshold 2
0x342A	CTRL_DPC_25_HCG	–	R	Bit[7]: Not used Bit[6:0]: Threshold 3
0x342B	CTRL_DPC_26_HCG	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 4
0x342C	CTRL_DPC_27_HCG	–	R	Bit[7:4]: Not used Bit[3:0]: Level
0x342D	CTRL_DPC_21_LCG	–	R	Bit[7]: Not used Bit[6:0]: Black thresholds
0x342E	CTRL_DPC_22_LCG	–	R	Bit[7:5]: Not used Bit[4:0]: White thresholds
0x342F	CTRL_DPC_23_LCG	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 1
0x3430	CTRL_DPC_24_LCG	–	R	Bit[7:6]: Not used Bit[5:0]: Threshold 2
0x3431	CTRL_DPC_25_LCG	–	R	Bit[7]: Not used Bit[6:0]: Threshold 3
0x3432	CTRL_DPC_26_LCG	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 4
0x3433	CTRL_DPC_27_LCG	–	R	Bit[7:4]: Not used Bit[3:0]: Level

4.5 HDR combine principle

figure 4-17 shows the principle of HDR combine.

- For linear mode, output data is 12 bit linear data.
- For HDR mode, the data output could be 16-bit linear data or both 12-bit HCG and LCG data. HCG and LCG can be combined inside the sensor or externally into 16-bit HDR data. The ratio between HCG and LCG is determined by conversion gain, analog gain, and digital gain.
- This ratio should not exceed 16. For example, if conversion gain is 10, (HCG_analog_gain x HCG_digital_gain)/(LCG_analog_gain x LCG_digital_gain) should not be greater than 1.6.

figure 4-17 HDR combine principle diagram

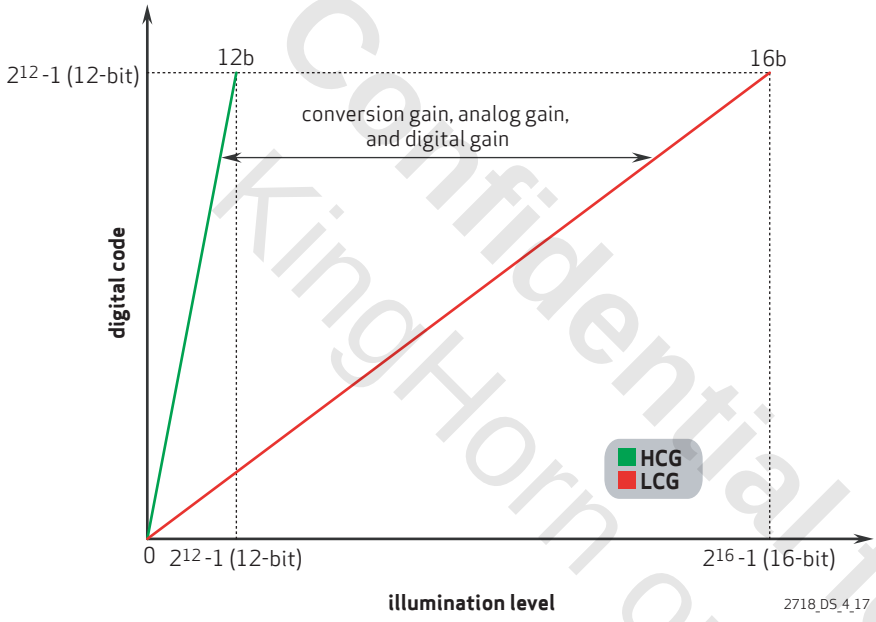


table 4-5 combine control registers

address	register name	default value	R/W	description
0x3250	ISP_DP_CONF1	0x33	RW	Bit[4]: comb_en DCG combine enable

5 image output interface

5.1 image output format

table 5-1 summarizes the output formats which the OV2718 supports.

table 5-1 image output format summary

format		description
linear	12b	12-bit RAW data, either HCG or LCG
HDR	2x12b DCG	{12-bit HCG} + {12-bit LCG}
	16b combined DCG	16-bit combined DCG data
	12b compressed combined DCG	12-bit data compressed from 16-bit combined DCG data

Register interface_control0 with address 0x3190[7:0] is used for interface control.

table 5-2 interface control register

address	register name	default value	R/W	description
0x3190	INTERFACE_CTRL0	0x07	RW	Bit[7]: channel_cfg Channel configuration Bit[6:5]: Reserved Bit[4]: no_comp When high, single 12-bit data are sent without compression Bit[3]: lin_enable Linear mode enable Bit[2]: Reserved Bit[1:0]: data_width 00: Not used 01: 2x12 10: Comb 12 11: Comb 16

table 5-3 represents the interface_ctrl0 setting for different output formats.

table 5-3 register setting for different output formats

format		register setting[a]			
		0x3190[1:0]data_width	0x3190[3] lin_enable	0x3190[5] 10b_mode	0x3190[7] channel_cfg
linear	12b	xx	1	0	x
HDR	2x12b DCG	01	0	0	0
	16b combined DCG	11	0	x	x
	12b compressed combined DCG	10	0	x	0

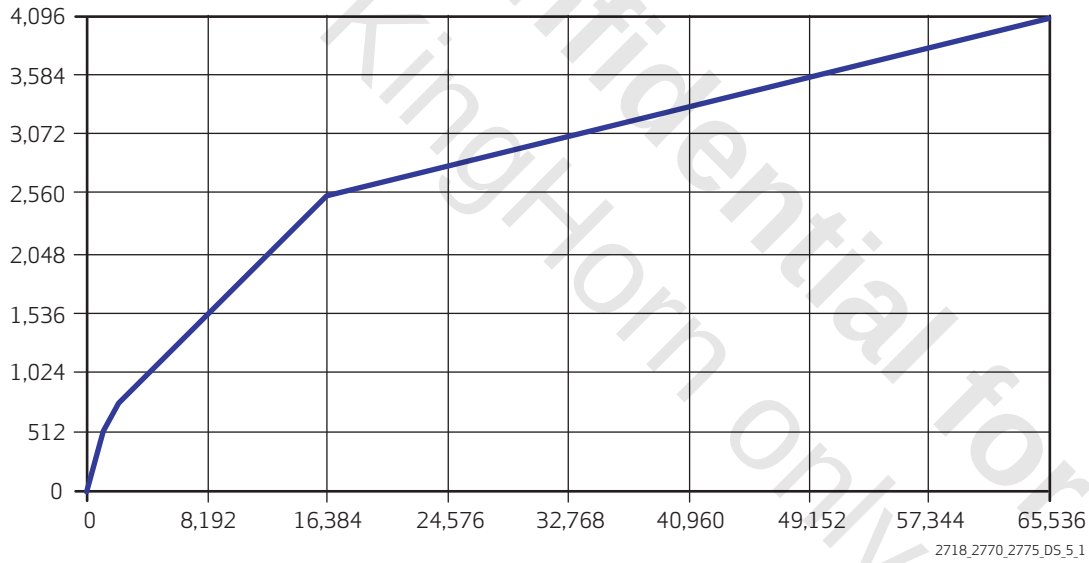
a. x means do not care

5.2 data compression algorithm

The OV2718 has a data compression from 16-bit to 12-bit by a 4-piece piece-wise linear (PWL) curve defined by the following formula and shown in **figure 5-1**.

$$y_{out\_12b} = \begin{cases} \frac{y_{in\_16b}}{2}, & y_{in\_16b} < 1024 \\ \frac{y_{in\_16b}}{4} + 256, & 1024 \le y_{in\_16b} < 2048 \\ \frac{y_{in\_16b}}{8} + 512, & 2048 \le y_{in\_16b} < 16384 \\ \frac{y_{in\_16b}}{32} + 2048, & y_{in\_16b} \ge 16384 \end{cases}$$

figure 5-1 16-bit to 12-bit PWL compression



The backend processor can decompress 12-bit data to 16-bit data using the following formula.

$$\mathbf{y_{out\_16b}} = \begin{cases} \mathbf{2 \times y_{in\_12b}} & \mathbf{y_{in\_12b} < 512} \\ \mathbf{4 \times (y_{in\_12b} - 256),} & \mathbf{512 \le y_{in\_12b} < 768} \\ \mathbf{8 \times (y_{in\_12b} - 512),} & \mathbf{768 \le y_{in\_12b} < 2560} \\ \mathbf{32 \times (y_{in\_12b} - 2048),} & \mathbf{y_{in\_12b} \ge 2560} \end{cases}$$

5.3 HDR output

The OV2718 supports MIPI, LVDS and DVP output interface, which will be described by the following sections.

5.3.1 MIPI

The MIPI interface supports 1, 2, or 4 lanes. The data output format is the same regardless of how many lanes are used with MIPI. The data packet illustrations in this section are to be interpreted line-wise as one consecutive data stream and show the layout of the data packet. The data packet is divided up between the lanes per byte (8 bits) according to MIPI CSI-2.

The OV2718 outputs multiple captures over virtual channels as shown in **figure 5-2**. Short-packets denote frame-start (FS) and frame-end (FE) on the respective virtual channel. If only one capture is output from the sensor, virtual channel 0 is used as default.

The OV2718 can also output multiple captures over the shared virtual channel, as shown in **figure 5-4** and **figure 5-5**. If a shared virtual channel is used, only one FS and FE packet will be sent per frame.

figure 5-2 HDR with MIPI virtual channel diagram

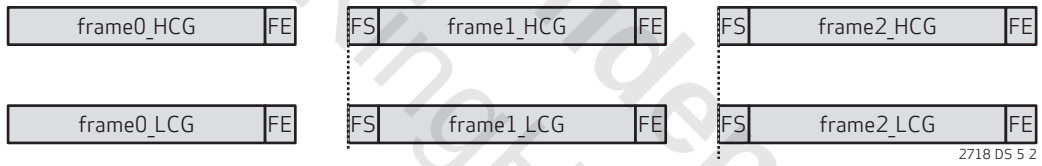


figure 5-3 HDR with MIPI virtual channel detail diagram

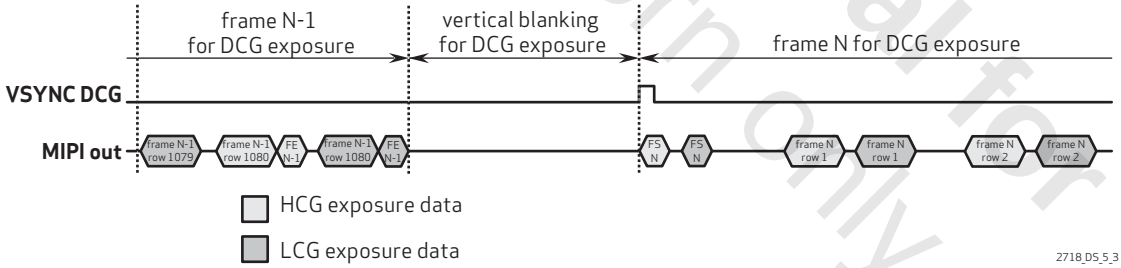


figure 5-4 HDR without MIPI virtual channel overview diagram

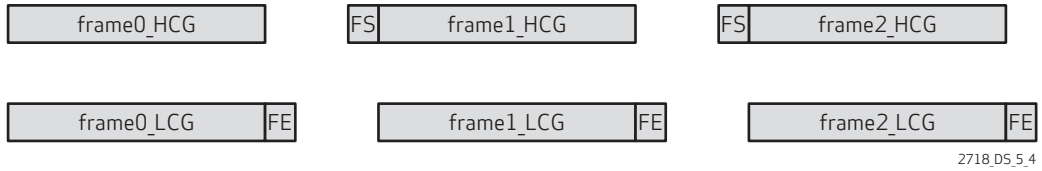


figure 5-5 HDR without MIPI virtual channel detail diagram

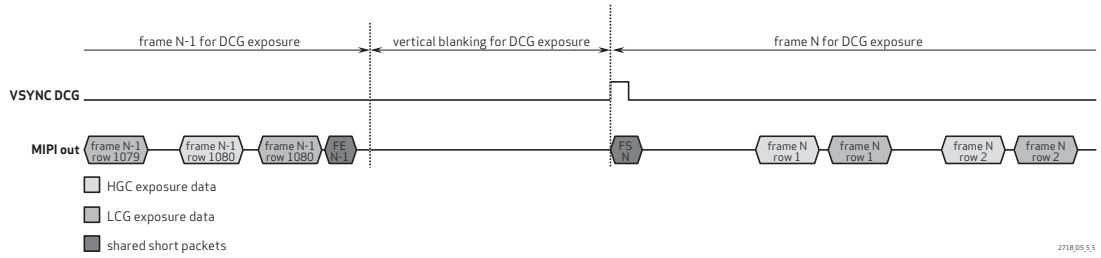


table 5-4 represents the resolution and maximum frame rate for MIPI with different output format.

table 5-4 supported output formats and frame rates for MIPI

maximum frame rate supported via MIPI (600 Mbps/lane) interface at 1920x1080		
format		maximum frame rate
linear	12b	30 fps
HDR	2x12b DCG	30 fps
	16b combined DCG	30 fps
	12b compressed combined DCG	30 fps

table 5-5 defines the default MIPI RAW image data type codes. The values are defined by the register listed in **table 5-5**.

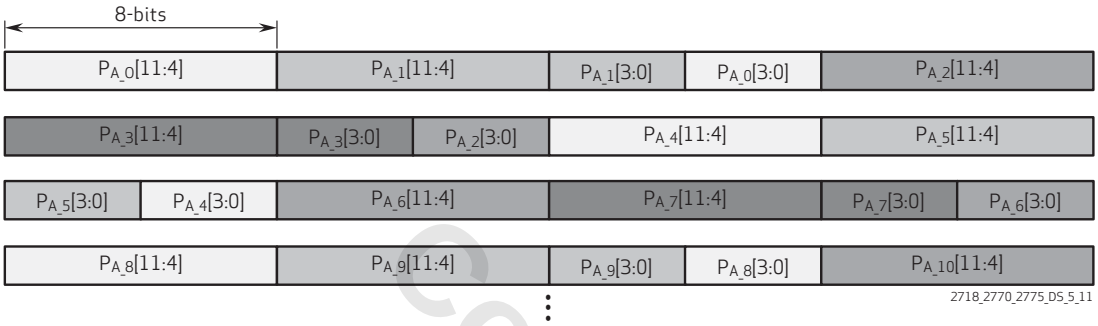
table 5-5 MIPI RAW image data types

default data type	register address	description
2C	0x3210	RAW 12
30	0x320E	RAW 16

5.3.1.1 12b linear mode

One value per pixel: P_A (12-bit RAW)

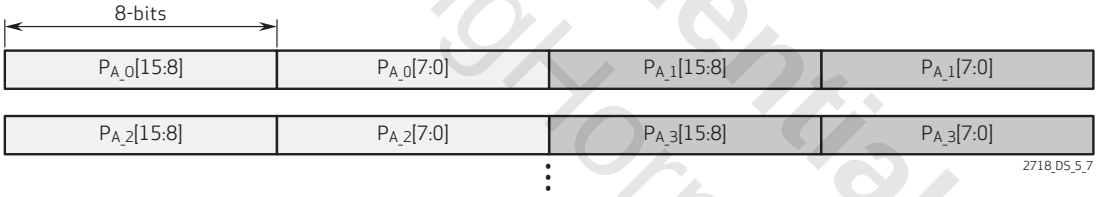
figure 5-6 12b linear mode diagram



5.3.1.2 16b combined DCG HDR

One value per pixel: P_A (16-bit combined DCG)

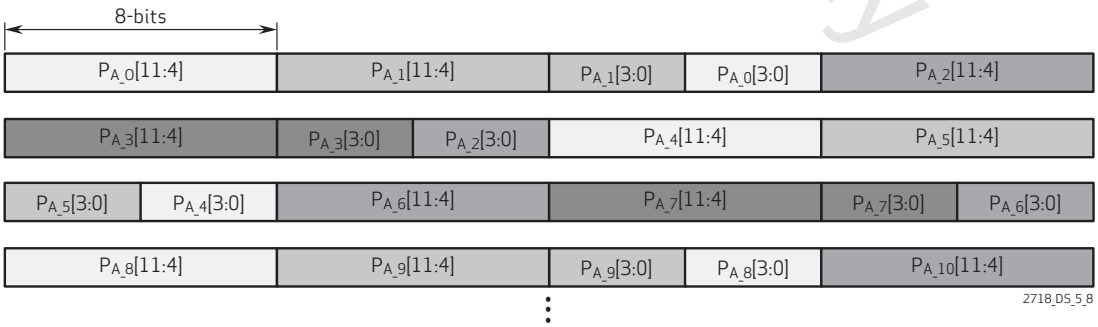
figure 5-7 16b combined DCG HDR diagram



5.3.1.3 12b compressed combined DCG HDR

One value per pixel: P_A (12-bit, compressed from 16-bit combined DCG)

figure 5-8 12b compressed DCG single HDR diagram



5.3.1.4 2x12b DCG HDR

Two values per pixel: P_A (12-bit HCG), P_B (12-bit LCG)

figure 5-9 2x12b DCG HDR diagram

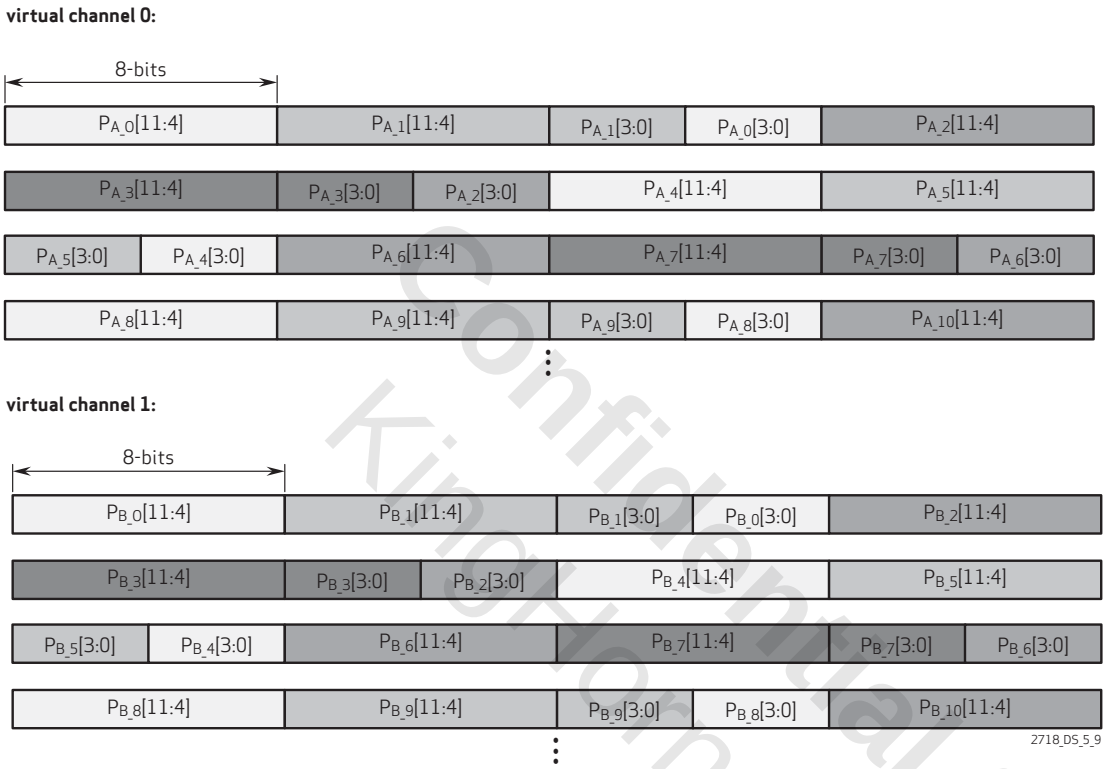


table 5-6 MIPI control registers (sheet 1 of 11)

address	register name	default value	R/W	description
0x31D0	CLK_POST_CONST_MIN	0x3C	RW	T(clk_post) Constant Minimum Value, Default Value: 60ns
0x31D1	CLK_POST_UI_MIN	0x34	RW	T(clk_post) UI Minimum Value, Default Value: 52 UIs
0x31D2	CLK_TRAIL_CONST_MIN	0x3C	RW	T(clk_trail) Constant Minimum Value, Default Value: 60ns
0x31D3	CLK_TRAIL_UI_MIN	0x00	RW	T(clk_trail) UI Minimum Value, Default Value: 0 UI
0x31D4	CLK_PREPARE_CONST_MIN	0x2D	RW	T(clk_prepare) Constant Minimum Value, Default Value: 38ns

table 5-6 MIPI control registers (sheet 2 of 11)

address	register name	default value	R/W	description
0x31D5	CLK_PREPARE_UI_MIN	0x00	RW	T(clk_prepare) UI Minimum Value, Default Value: 0 UIs
0x31D6	CLK_ZERO_CONST_MIN1	0x01	RW	T(clk_zero) Constant Minimum Value (high 2 bits)
0x31D7	CLK_ZERO_CONST_MIN2	0x06	RW	T(clk_zero) Constant Minimum Value (low 8 bits) Default Value: 44ns
0x31D8	CLK_ZERO_UI_MIN	0x00	RW	T(clk_zero) UI Minimum Value Default Value: 0 UIs
0x31D9	HS_EXIT_CONST_MIN	0x64	RW	T(hs_exit) Constant Minimum Value Default Value: 100ns
0x31DA	HS_EXIT_UI_MIN	0x00	RW	T(hs_exit) UI Minimum Value Default Value: 0 UI
0x31DB	HS_PREPARE_CONST_MIN	0x28	RW	T(hs_prepare) Constant Minimum Value Default Value: 40ns
0x31DC	HS_PREPARE_UI_MIN	0x04	RW	T(hs_prepare) UI Minimum Value Default Value: 4 UI
0x31DD	HS_ZERO_CONST_MIN	0x69	RW	T(hs_zero) Constant Minimum Value Default Value: 105ns
0x31DE	HS_ZERO_UI_MIN	0x0A	RW	T(hs_zero) UI Minimum Value Default Value: 6 UI
0x31DF	HS_TRAIL_CONST_MIN	0x3C	RW	T(hs_trail) Constant Minimum Value Default Value: 65ns
0x31E0	HS_TRAIL_UI_MIN	0x04	RW	T(hs_trail) UI Minimum Value Default Value: 4 UI
0x31E1	LPX_CONST_MIN	0x32	RW	T(lpx) Constant Minimum Value Default Value: 50ns
0x31E2	LPX_UI_MIN	0x00	RW	T(lpx) UI Minimum Value Default Value: 0 UI
0x31E3	MIPI_CLK_PERIOD1	0x00	RW	Clock Period of mipi_clk Used to calculate timing parameters of MIPI TX (low 2 bits, fraction) Default Value: 2'b00
0x31E4	MIPI_CLK_PERIOD2	0x08	RW	Clock Period of mipi_clk Used to calculate timing parameters of MIPI TX (high 8 bits, integer) 8.00ns

table 5-6 MIPI control registers (sheet 3 of 11)

address	register name	default value	R/W	description
0x31E5	MIPI_LANE_CTRL0	0x92	RW	Bit[7]: ext_timing Finish lane transfer long packet data exactly 0: Not used 1: Do not send any dummy data in data lane, meaning trail data will be behind image data i Bit[6]: clk_data_chg Clock lane data change, 2'b01 -> 2'b10 Bit[5]: dis_clk_lane (active high) Disable clock lane Bit[4]: line_sync_en Insert LS/LE in the MIPI TX stream if this bit is set Bit[3]: frame_cnt_zero_c1 MIPI TX channel 1 will keep frame counter zero if this bit is set Bit[2]: frame_cnt_zero_c0 MIPI TX channel 0 will keep frame counter zero if this bit is set Bit[1]: gate_clk_en2 (active high) Gate clock for clock lane when frame blanking time Bit[0]: gate_clk_en1 (active high) Gate clock for clock lane when line/frame blanking time
0x31E6	MIPI_LPKT_MAN	0x00	RW	Bit[7]: Reserved Bit[6]: lpkt_man_en Long packet manual input Bit[5:0]: dt_man Manual data type
0x31E7	MIPI_DI0	0x30	RW	Bit[7:6]: vc_num0 Virtual channel ID for data path 0 Bit[5:0]: img_dt0 Data type for data path 0
0x31E8	MIPI_DI1	0x6C	RW	Bit[7:6]: vc_num1 Virtual channel ID for data path 0 Bit[5:0]: img_dt1 Data type for data path 0
0x31E9	MIPI_DI2	0xAC	RW	Bit[7:6]: vc_num2 Virtual channel ID for data path 0 Bit[5:0]: img_dt2 Data type for data path 0

table 5-6 MIPI control registers (sheet 4 of 11)

address	register name	default value	R/W	description
0x31EA	MIPI_DI3	0xEC	RW	Bit[7:6]: vc_num3 Virtual channel ID for data path 0 Bit[5:0]: img_dt3 Data type for data path 0
0x31EB	MIPI_EMB	0x7F	RW	Bit[7]: Not used Bit[6]: use_emb_data_type Use embedded data type for embedded data rows Bit[5:0]: emb_dt Data type for embedded data
0x31EC	MIPI_IMG_WIDTHH0	0x0F	RW	Bit[7:0]: img_width[15:8] Channel 0 image width
0x31ED	MIPI_IMG_WIDTHL0	0x20	RW	Bit[7:0]: img_width[7:0] Channel 0 image width
0x31EE	MIPI_IMG_HEIGHTH0	0x04	RW	Bit[7:0]: img_height[15:8] Channel 0 image height
0x31EF	MIPI_IMG_HEIGHTL0	0x48	RW	Bit[7:0]: img_height[7:0] Channel 0 image height
0x31F0	MIPI_IMG_WIDTH1_H	0x07	RW	Bit[7:0]: img_width[15:8] Channel 1 image width
0x31F1	MIPI_IMG_WIDTH1_L	0x90	RW	Bit[7:0]: img_width[7:0] Channel 1 image width
0x31F2	MIPI_IMG_HEIGHTH1	0x04	RW	Bit[7:0]: img_height[15:8] Channel 1 image height
0x31F3	MIPI_IMG_HEIGHT1_L	0x48	RW	Bit[7:0]: img_height[7:0] Channel 1 image height
0x31F4	MIPI_IMG_WIDTH2_H	0x07	RW	Bit[7:0]: img_width[15:8] Channel 2 image width
0x31F5	MIPI_IMG_WIDTH2_L	0x90	RW	Bit[7:0]: img_width[7:0] Channel 2 image width
0x31F6	MIPI_IMG_HEIGHT2_L	0x04	RW	Bit[7:0]: img_height[15:8] Channel 2 image height
0x31F7	MIPI_IMG_HEIGHT2_L	0x48	RW	Bit[7:0]: img_height[7:0] Channel 2 image height
0x31F8	MIPI_IMG_WIDTH3_H	0x07	RW	Bit[7:0]: img_width[15:8] Channel 3 image width
0x31F9	MIPI_IMG_WIDTH3_L	0x90	RW	Bit[7:0]: img_width[7:0] Channel 3 image width

table 5-6 MIPI control registers (sheet 5 of 11)

address	register name	default value	R/W	description
0x31FA	MIPI_IMG_HEIGHT3_H	0x04	RW	Bit[7:0]: img_height[15:8] Channel 3 image height
0x31FB	MIPI_IMG_HEIGHT3_L	0x48	RW	Bit[7:0]: img_height[7:0] Channel 3 image height
0x31FC	MIPI_STATUS	–	R	Bit[7:2]: Not used Bit[1]: mipi_ph_done MIPI has transferred long packet header data. User can modify data type. Bit[0]: mipi_busy MIPI is transmitting data if this bit is asserted

table 5-6 MIPI control registers (sheet 6 of 11)

address	register name	default value	R/W	description
0x31FD	MIPI_LANE_CTRL1	0xCB	RW	Bit[7]: hs_zero_sync_en 0: Send 'hs_en' one cycle ahead of hs_zero state 1: Send 'hs_en' sync with hs_zero state Bit[6]: sof_send_fs Send "FS" packet after MIPI received SOF 0: Send "FS" packet when VFIFO data is ready 1: Send "FS" packet when MIPI received SOF Bit[5]: chksum_exchg Long packet checksum byte exchange enable 0: Checksum = CRC[15:0] 1: Checksum = {CRC[7:0], CRC[15:8]} Bit[4]: Reserved Bit[3]: lp_state Low power state when data lane is idle 0: Low power signal for each 1: lp_p or lp_n will stay "1" if the current data lane is not active Bit[2]: pclk_inv_en (active high) PCLK inverse enable (output to PHY) Bit[1]: gen_fe_en1 Force to generate frame end short packet in channel 1 when MIPI TX has transmitted one line if VFIFO of this channel is overflow Bit[0]: gen_fe_en0 Force to generate frame end short packet in channel 0 when MIPI TX has transmitted one line if VFIFO of this channel is overflow

table 5-6 MIPI control registers (sheet 7 of 11)

address	register name	default value	R/W	description
0x31FE	MIPI_LANE_CTRL2	0x0F	RW	Bit[7]: d4_inv_en Data lane 4 inverse enable Bit[6]: d3_inv_en Data lane 3 inverse enable Bit[5]: d2_inv_en Data lane 2 inverse enable Bit[4]: d1_inv_en Data lane 1 inverse enable Bit[3]: lane4_en Data lane 4 enable Bit[2]: lane3_en Data lane 3 enable Bit[1]: lane2_en Data lane 2 enable Bit[0]: lane1_en Data lane 1 enable

table 5-6 MIPI control registers (sheet 8 of 11)

address	register name	default value	R/W	description
0x31FF	MIPI_LANE_CTRL3	0x03	RW	Bit[7]: ch3_crop_en Channel 3 crop enable 0: Channel 3 crop disable 1: Channel 3 crop enable Bit[6]: ch2_crop_en Channel 2 crop enable 0: Channel 2 crop disable 1: Channel 2 crop enable Bit[5]: ch1_crop_en Channel 1 crop enable 0: Channel 1 crop disable 1: Channel 1 crop enable Bit[4]: ch0_crop_en Channel 0 crop enable 0: Channel 0 crop disable 1: Channel 0 crop enable Bit[3]: fcnt_zero_c3 MIPI TX channel 3 will keep frame counter zero if this bit is set Bit[2]: fcnt_zero_c2 MIPI TX channel 2 will keep frame counter zero if this bit is set Bit[1]: gen_fe_en3 Force to generate frame end short packet in channel 3 when MIPI TX has transmitted one line if VFIFO of this channel is overflow Bit[0]: gen_fe_en2 Force to generate frame end short packet in channel 2 when MIPI TX has transmitted one line if VFIFO of this channel is overflow

table 5-6 MIPI control registers (sheet 9 of 11)

address	register name	default value	R/W	description
0x3200	MIPI_TST_MODE	0x00	RW	Bit[7:6]: Not used Bit[5]: lp_n_man_data Output manual lower power data in MIPI TX test mode Bit[4]: lp_p_man_data Output manual lower power data in MIPI TX test mode Bit[3]: lp_man_en Output manual low power data enable in low power test mode and de-assert high speed signal (hs_en or valid) Bit[2]: hs_man_en Manual test data will output to PHY when this bit is set and MIPI TX in high speed test mode (reg25 must be set in this case) Bit[1]: tst_mode 0: Test start point sync by "mipi_test" 1: Test start point sync by MIPI RX "prbs_en" Bit[0]: mipi_tst (active high) Test MIPI TX and RX PHY
0x3201	MANUAL_TST_DATA	0xFF	RW	Manual Test Data for MIPI PHY
0x3202	MIPI_TST_CFG	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rx_prbs_en Enable MIPI PHY test including RX PHY and TX PHY
0x3203	MAX_FRAME_CNT0_H	0xFF	RW	High Byte of Maximum Frame Counter of Channel 0
0x3204	MAX_FRAME_CNT0_L	0xFF	RW	Low Byte of Maximum Frame Counter of Channel 0
0x3205	MAX_FRAME_CNT1_H	0xFF	RW	High Byte of Maximum Frame Counter of Channel 1
0x3206	MAX_FRAME_CNT1_L	0xFF	RW	Low Byte of Maximum Frame Counter of Channel 1
0x3207	MAX_FRAME_CNT2_H	0xFF	RW	High Byte of Maximum Frame Counter of Channel 2
0x3208	MAX_FRAME_CNT2_L	0xFF	RW	Low Byte of Maximum Frame Counter of Channel 2
0x3209	MAX_FRAME_CNT3_H	0xFF	RW	High Byte of Maximum Frame Counter of Channel 3

table 5-6 MIPI control registers (sheet 10 of 11)

address	register name	default value	R/W	description
0x320A	MAX_FRAME_CNT3_L	0xFF	RW	Low Byte of Maximum Frame Counter of Channel 3
0x320E	RAW16	0x30	RW	RAW16 Data Type
0x3210	RAW12	0x2C	RW	RAW12 Data Type
0x3211	RAW10	0x2B	RW	RAW10 Data Type
0x3215	DAT_SEQ_CTRL	0x00	RW	Bit[7:5]: total_seq RGB sequence 000: Sequence = 'BGR' 001: Sequence = 'BRG' 010: Sequence = 'GBR' 011: Sequence = 'GRB' 100: Sequence = 'RGB' Bit[4:3]: high_half_seq Quarter sequence Used to adjust the each 12-bits data sequence 00: data[11:0] 01: {data[9:0],data[11:10]} 10: {data[7:0],data[11:8]} 11: Not used Bit[2]: low_half_seq Low half sequence Used to adjust the low 24-bits data Sequence = 1'b0, data[23:0], = 1'b1, {data[11:0], data[23:12]} Bit[1]: quarter_seq High half sequence Used to adjust the low 24-bits data sequence = 1'b0, data[47:24], = 1'b1, {data[35:24], data[47:36]} Bit[0]: rgb_seq Total sequence = 1'b0, data[47:0], = 1'b1, {data[11:0], data[23:12], data[35:24], data[47:36]}
0x3216	LP_DELAY	0x04	RW	LP00--LP11 Delay Cycle When hs_zero Sync Enable
0x3217	MIPI_DATA_TAG0	0x30	RW	Data_ID Tag Transmitted in Virtual Channel 0 for Supporting "Same Image Data Transmit in Different Virtual Channel With Different Data_ID Tag

table 5-6 MIPI control registers (sheet 11 of 11)

address	register name	default value	R/W	description
0x3218	MIPI_DATA_TAG1	0x6C	RW	Data_ID Tag Transmitted in Virtual Channel 1 for Supporting "Same Image Data Transmit in Different Virtual Channel With Different Data_ID Tag
0x3219	MIPI_DATA_TAG2	0xAC	RW	Data_ID Tag Transmitted in Virtual Channel 2 for Supporting "Same Image Data Transmit in Different Virtual Channel With Different Data_ID Tag
0x321A	MIPI_DATA_TAG3	0xEC	RW	Data_ID Tag Transmitted in Virtual Channel 3 for Supporting "Same Image Data Transmit In Different Virtual Channel With Different Data_ID Tag
0x321B	USE_VFIFO_TYPE	0x01	RW	Use Size Signals (12, 10, and 8) from VFIFO

5.3.2 LVDS

figure 5-10 HDR with LVDS dedicated lane (4-lane) diagram

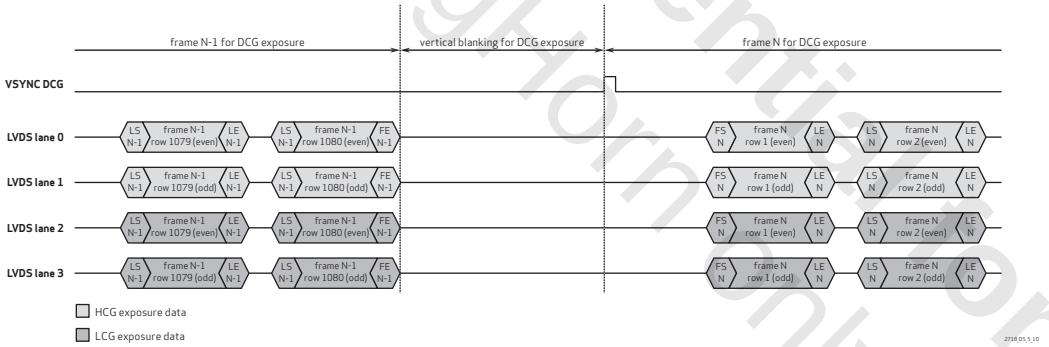


figure 5-11 HDR with LVDS dedicated lane (2-lane) diagram

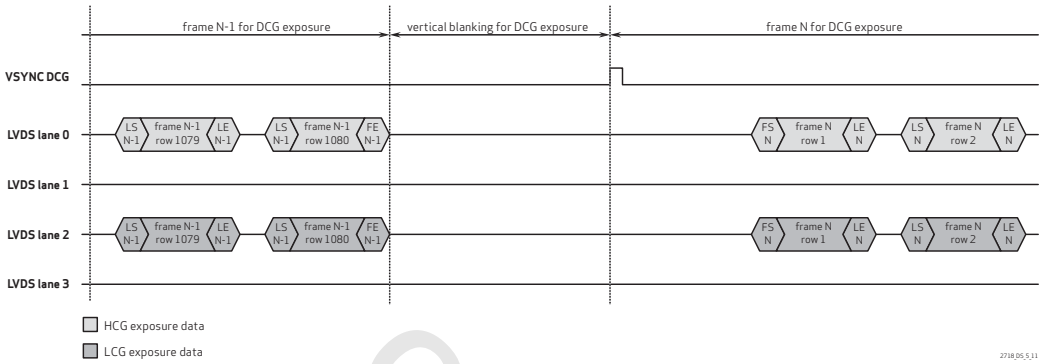


table 5-7 represents the resolution and maximum frame rate for LVDS with different output format.

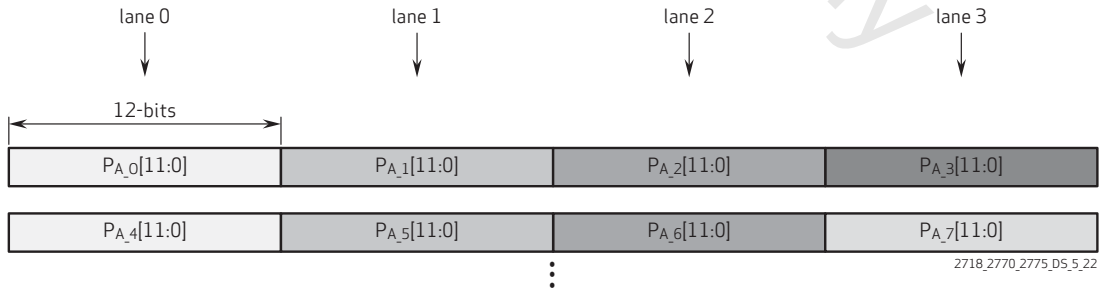
5.3.2.1 12 bits linear mode

table 5-7 supported output formats and frame rates for LVDS

maximum frame rate supported via LVDS (600 Mbps/lane) interface at 1920x1080		
format		maximum frame rate
linear	12b	30 fps
HDR	2x12b DCG	30 fps
	16b combined DCG	30 fps
	12b compressed combined DCG	30 fps

One value per pixel: P_A (12-bit RAW)

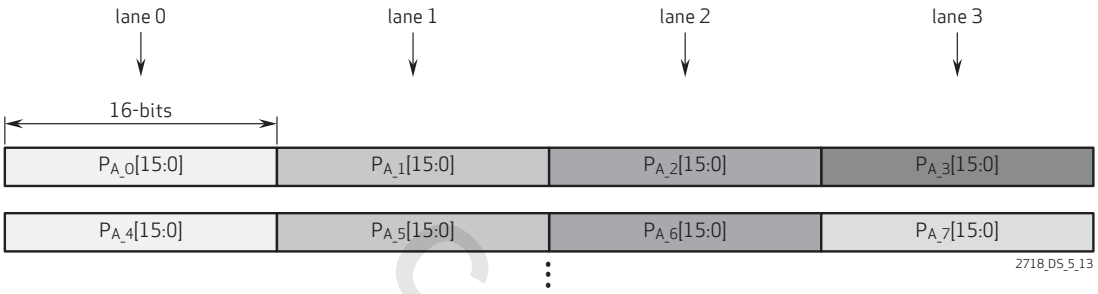
figure 5-12 12 bits linear mode diagram



5.3.2.2 16b combined DCG HDR

One value per pixel: P_A (16-bit combined DCG)

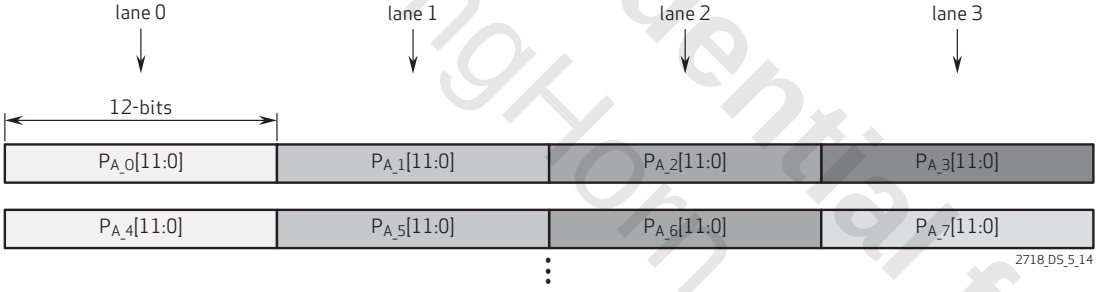
figure 5-13 16b combined DCG HDR diagram



5.3.2.3 12b compressed combined DCG HDR

One value per pixel: P_A (12-bit, compressed from 16-bit)

figure 5-14 12b compressed combined DCG HDR diagram



5.3.2.4 2x12b DCG HDR

Two values per pixel: P_A (12-bit HCG), P_B (12-bit LCG)

figure 5-15 2x12b DCG HDR diagram

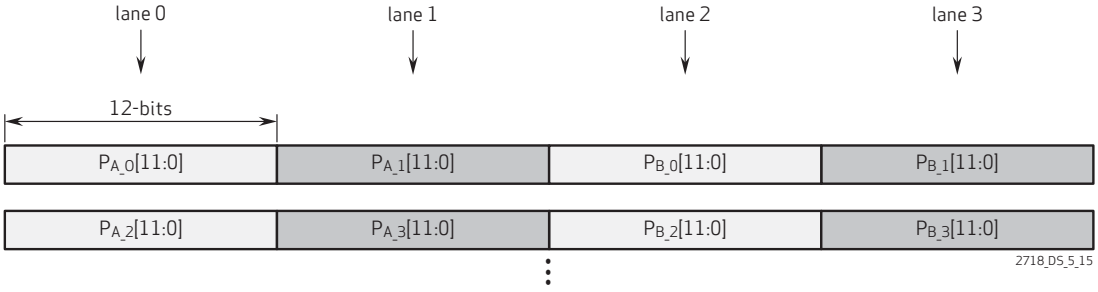


table 5-8 LVDS control registers

address	register name	default value	R/W	description
0x3230	LVDS_R0	0x2A	RW	Bit[7]: Not used Bit[6]: sync_cod_man Sync code manual enable Bit[5]: syncd_en Bit[4]: lvds_pclk_inv Invert LVDS pclk_o Bit[3]: r_chid_en Channel ID enable in sync per lane mode Bit[2]: lvds_f CCIR parameter F Bit[1]: sav_first_en 0: EAV first 1: SAV first Bit[0]: sync_code_mod (fixed to 1) Sync code per lane
0x3231	LVDS_R2	0x00	RW	Dummy Data0 High Nibble
0x3232	LVDS_R3	0x80	RW	Dummy Data0 Low Byte
0x3233	LVDS_R4	0x00	RW	Dummy Data1 High Nibble
0x3234	LVDS_R5	0x10	RW	Dummy Data1 Low Byte
0x3235	LVDS_R6	0xAA	RW	frame_st
0x3236	LVDS_R7	0x55	RW	frame_ed
0x3237	LVDS_R8	0x99	RW	line_st
0x3238	LVDS_R9	0x66	RW	line_ed
0x3239	LVDS_RA	0x08	RW	Bit[7:4]: Not used Bit[3]: bit_flip Bit[2]: Not used Bit[1]: ln2_sel Bit[0]: Not used
0x323A	LVDS_RB	0x88	RW	Bit[7]: sleep_en Bit[6]: Not used Bit[5]: frame_rst_en Bit[4:0]: ln_end_dly
0x323B	LVDS_RC	0x00	RW	r_blk_time High Nibble
0x323C	LVDS_RD	0x00	RW	r_blk_time Low Byte
0x323D	LVDS_LANE_NR	0x03	RW	Number of Active LVDS Lanes

5.3.3 DVP

The OV2718 can output pixel data on a 12-bit DVP bus. In DVP mode, VSYNC indicates start of DCG (HCG/LCG)-exposure output and HREF indicates that pixel data is output on DVP (HCG/LCG).

HREF, VSYNC, and PCLK are configured as video output port by default as shown in **figure 5-16**. The leading edge of VSYNC is triggered by an internal SOF signal and the interval between the internal SOF signal and VSYNC is controlled by v_sync_delay (0x31B4~0x31B6 in unit of PCLK periods). VSYNC pulse width is set by registers 0x31B0~0x31B3 as in the following formula:

VSYNC width = [VSYNC width line × t_{Row}] + [VSYNC width pixel × t_{PCLK}]

where:

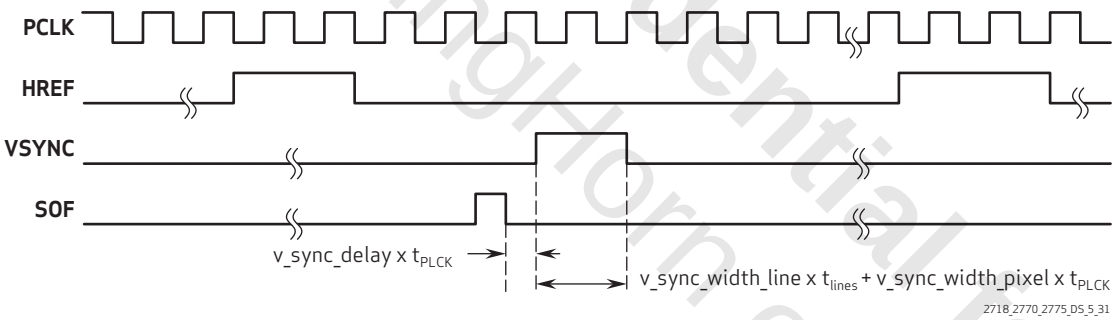
t_{Row} is row period

t_{PCLK} is PCLK period

VSYNC width line - {0x31B0, 0x31B1}

VSYNC width pixel - {0x31B2, 0x31B3}

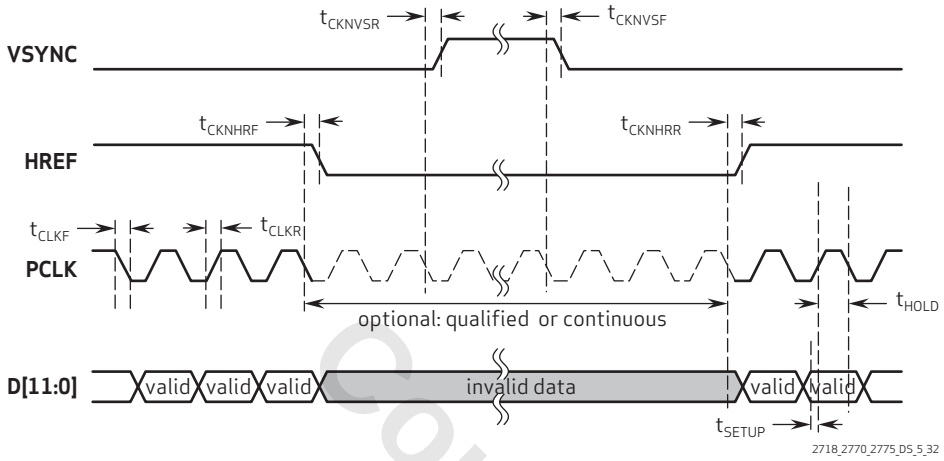
figure 5-16 DVP diagram



The OV2718 supports walking one test pattern to test the connection between the sensor and the backend processor. The test pattern is enabled by register 0x31B8[0]. By default, the image data bits are aligned with pins D[11:0].

The driver strength of the DVP can be configured by 0x3488[1:0].

figure 5-17 DVP setup/hold time diagram



The DVP output is qualified by VSYNC and HREF and the timing is shown in **figure 5-18**.

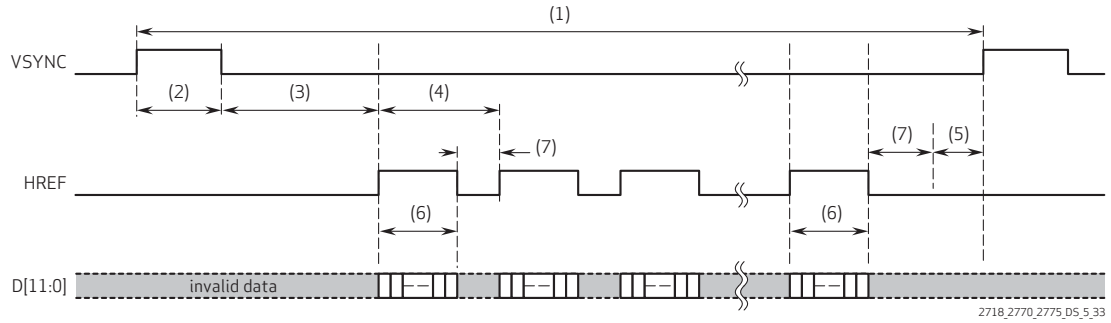
table 5-9 DVP setup/hold time[ab]

symbol	parameter	min	typ	max	unit
t_{CKNVSR}	PCLK falling edge to VSYNC rising edge delay	–	0.07	–	ns
t_{CKNVSF}	PCLK falling edge to VSYNC falling edge delay	–	0.49	–	ns
t_{CKNHRF}	PCLK falling edge to HREF falling edge delay	–	-0.29	–	ns
t_{CKNHRR}	PCLK falling edge to HREF rising edge delay	–	-0.61	–	ns
t_{CLKF}	PCLK fall time	–	1.08	–	ns
t_{CLKR}	PLCK rise time	–	1.93	–	ns
t_{SETUP}	data setup time	5.07	5.60	6.20	ns
t_{HOLD}	data hold time	6.20	6.60	6.73	ns

a. measured at 1.8V DOVDD and 75 MHz PCLK, with 2x drive strength

b. timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 90%

figure 5-18 DVP timing diagram



(1) frame period

(2) VSYNC width

(3) VSYNC to HREF

(4) line period

(5) HREF to VSYNC

(6) active pixel

(7) horizontal blanking

(8) last horizontal blanking to VSYNC high

VSYNC pulse width is programmable from 1 CLK to 1 frame (high period = #lines + #pixels): registers 0x31B0~0x31B1: #lines, registers 0x31B2~0x31B3: #pixels

N = VS-delay in whole rows × image width

Height = rows × image width

table 5-10 represents the resolution and maximum frame rate for DVP with different output format.

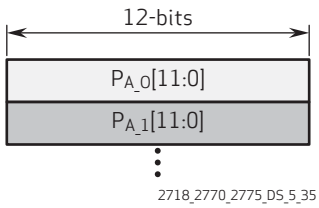
table 5-10 supported output formats and frame rates for DVP

maximum frame rate supported via DVP 900 Mbps interface at 1920x1080		
format		maximum frame rate
linear	12b	30 fps
HDR	12b compressed combined DCG	30 fps

5.3.3.1 12 bits linear mode

One value per pixel: P_A (12-bit RAW)

figure 5-19 12 bits linear mode diagram



5.3.3.2 12b compressed combined DCG HDR

One value per pixel: P_A (12-bit, compressed from 16-bit)

figure 5-20 12b compressed combined DCG HDR diagram

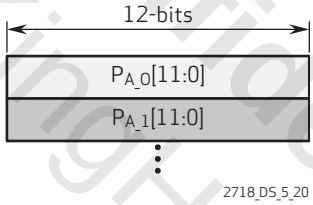


table 5-11 DVP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x31B0	VSYNC_WIDTH_LINE_H	0x00	RW	VSYNC Width by Line Number High Byte
0x31B1	VSYNC_WIDTH_LINE_L	0x00	RW	VSYNC Width by Line Number Low Byte
0x31B2	VSYNC_WIDTH_PIXEL_H	0x02	RW	VSYNC Width by Pixel Number High Byte
0x31B3	VSYNC_WIDTH_PIXEL_L	0x00	RW	VSYNC Width by Pixel Number Low Byte, Must Be Larger Than 0
0x31B4	VSYNC_DELAY_H	0x00	RW	VSYNC Delay Count High Byte
0x31B5	VSYNC_DELAY_M	0x01	RW	VSYNC Delay Count Mid Byte
0x31B6	VSYNC_DELAY_L	0x00	RW	VSYNC Delay Count Low Byte

table 5-11 DVP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x31B7	POLARITY_CTRL	0x00	RW	Bit[7]: Reserved Bit[6]: Bit reverse enable Bit[5]: vsync_gate_clk_enable Bit[4]: href_gate_clk_enable Bit[3]: Reserved Bit[2]: href_polarity Bit[1]: vsync_polarity Bit[0]: pclk_polarity Also PCLK gate low enable
0x31B8	BIT_ORDER	0x00	RW	Bit[7:4]: Reserved Bit[3]: bit_test_mode Bit[2]: bit_test_bit10 Bit[1]: bit_test_bit8 Bit[0]: bit_test_enable
0x31B9	BYP_SELECT	0x00	RW	Bit[7:6]: Reserved Bit[5]: data_bit_shift Bit[4]: href_sel Bit[3:0]: bypass_sel
0x31BA	R_FIFO	0x00	RW	Top Sync FIFO Control

5.4 register writing

5.4.1 suggestion for writing register value just after VSYNC or FS

In order to avoid register setting for one frame being split into two frames by mistake, the register value should be written as early as possible after VSYNC or FS. The register value written in frame N will take effect in frame N+2.

5.5 embedded data

Additional information about the set up and configuration of the sensor can be embedded in the video stream. The embedded data contains the values of a programmable list of registers to describe the current state of the sensor (e.g., frame counter, exposure time and gain, etc.). The embedded data is added before the video stream. Embedded data can be displayed in the image using register 0x30C1[2]. When embedded data is enabled, vertical crop start address (0x30A2, 0x30A3) and output size (0x30AE, 0x30AF) must be increased by 2.

Embedded data will be read using a specific read bus from the registers. The normal register bus will not be used since it will be occupied.

In linear mode, only one row embedded data is supported. Row two will be blank data.

5.5.1 embedded data format at output

Each register value is preceded by the tag 0xDA. When output data width is more than 8 bits, tag and register values will be MSB aligned.

In HDR mode, embedded data is added to the HCG channel in 2x12 mode. Embedded row data will be blank in the LCG capture.

The number of registers transmitted is dependent on the register start and end address and might be one or two rows. The last four registers are CRC value (4 bytes) preceded with the tag value before each byte. The range of registers, selected as embedded data, will be output in incrementing order from start to end address. The embedded data row will automatically continue on the next row. When the whole range has been output, the CRC data will be appended. If the requested range does not fit within two embedded data rows, the range will be truncated with an appended CRC value. If CRC3 is not the end of the embedded rows, it will be terminated with 'h00.

5.5.1.1 bit alignment

12 bits data (DCG compressed or linear mode):

{Embedded data, 4'h0}

16 bits data (data packed as 2x8 bits words):

{Embedded data, 8'h0}

figure 5-21 embedded data layout diagram

table 5-12 embedded data registers

address	register name	default value	R/W	description
0x3468	EMB_START_ADDR0_H	0x30	RW	High Address for the First Embedded Data Range 0
0x3469	EMB_START_ADDR0_L	0x00	RW	Low Address for the First Embedded Data Range 0
0x346A	EMB_END_ADDR0_H	0x35	RW	High Address for the Last Embedded Data Range 0
0x346B	EMB_END_ADDR0_L	0x00	RW	Low Address for the Last Embedded Data Range 0

5.6 group hold

The OV2718 supports a group hold function where the register values are recorded in an internal buffer instead of writing to the register directly.

The OV2718 supports up to four groups. The number of entries for each group is set by registers 0x3460~0x3463. The total sum for the four groups is limited to 256 registers. In manual mode, a register write burst can be triggered with a SCCB write and the specified group's register settings will be written to the register interface. In automatic mode, two groups are selected and the number of frames each group should be active. The sensor will continuously update the register settings accordingly.

The group hold function is controlled through registers 0x3460~0x346D.

To program group hold, set 0x3467 to 0x00 and select which group to program in 0x3464[3:2]. Then, specify the register to group hold by entering the register address and swap MSB (bit[15]) in address to 1. So, 0x3000 would be 0xB000, 0x30E6 would be 0xB0E6, etc.

To enable group hold, set register 0x3467[1:0] for 'single launch' to launch group settings once, or 'auto launch' to automatically switch between groups selected in 0x3464[3:0].

group hold examples:

- set group0

```
6c 3467 00;
6c 3464 00; select group 0 for record
6c b0b6 1; record registers for group launch by setting bit[15] of address to 1
```

- set group1

```
6c 3467 00;
6c 3464 04; select group 1 for record
6c b0b6 2;
```

- set group2

```
6c 3467 00;
6c 3464 08; select group 2 for record
6c b0b6 3;
  -  set group3
6c 3467 00;
6c 3464 0c; select group 3 for record
6c b0b6 4;
  -  single launch group0
6c 3464 10;
6c 3467 01; single launch
  -  single launch group1
6c 3464 14;
6c 3467 01
  -  single launch group2
6c 3464 18;
6c 3467 01;
  -  single launch group3
6c 3464 1c;
6c 3467 01;
  -  auto switch between group0 and group1
6c 3464 11; group0 and 1
6c 3467 02; auto launch
  -  auto switch between group0 and group2
6c 3464 12; group 0 and 2
6c 3467 02; auto launch
  -  auto switch between group2 and group3
6c 3464 1b; group 2 and 3
6c 3467 02; auto launch
```

table 5-13 group hold control registers

address	register name	default value	R/W	description
0x3460	GROUP_LENGTH0	0x40	RW	Number of Registers for Group 0, Total Sum of 4 Groups Is Limited to 256
0x3461	GROUP_LENGTH1	0x40	RW	Number of Registers for Group 1
0x3462	GROUP_LENGTH2	0x40	RW	Number of Registers for Group 2
0x3463	GROUP_LENGTH3	0x40	RW	Number of Registers for Group 3
0x3464	GROUP_CTRL	0x03	RW	Bit[7]: Not used Bit[6]: launch_now Launch immediately when single_start is set Bit[5]: launch_pre_sof Launch before sensor core SOF, if single_start is set Bit[4]: launch_post_sof Launch after sensor core SOF, if single_start is set Bit[3:2]: first_grp_sel Main group select for hold and launch operation. Also used as the first group in auto mode. Bit[1:0]: second_grp_sel Used as second group in auto mode
0x3465	FIRST_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by First Group Select
0x3466	SECOND_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by Second Group Select
0x3467	OPERATION_CTRL	0x02	RW	Bit[7:2]: Not used Bit[1]: auto_mode Switches automatically between first and second groups using frame counts Bit[0]: single_start Launch only once. Reset by logic after done. Overridden by auto_mode.
0x3468	EMB_START_ADDR0_H	0x30	RW	High Address for the First Embedded Data Range 0
0x3469	EMB_START_ADDR0_L	0x00	RW	Low Address for the First Embedded Data Range 0
0x346A	EMB_END_ADDR0_H	0x35	RW	High Address for the Last Embedded Data Range 0
0x346B	EMB_END_ADDR0_L	0x00	RW	Low Address for the Last Embedded Data Range 0
0x346C	ACTIVE_GROUP_NR	–	R	Indicates Which Group is Active
0x346D	FRAME_CNT_ACTIVE	–	R	Number of Frames With the Current Group Valid Only in Auto Mode

5.7 cyclic redundancy check

The OV2718 supports cyclic redundancy check (CRC-32C) on the embedded data and SCCB (CRC-16-IBM) communication.

5.7.1 embedded data

The CRC on embedded data is calculated using CRC-32C. The polynomials are 0x1EDC6F41 (normal). The last four registers are CRC value (4 bytes) preceded with tag value before each byte. The tag (0xDA) is not included in the CRC.

5.7.2 SCCB communication

The CRC on SCCB write is calculated using CRC-16-IBM. The polynomial is 0x8005. CRC is calculated on both the (register) address and data (in the order of 1: high address byte, 2: low address byte 3: data). An SCCB read operation to any of the CRC registers (0x7FF6, 0x7FF7) will reset the CRC calculation. The CRC registers will be reset on the next SCCB write operation (i.e., they will hold the result of the previous CRC calculation until a new SCCB write occurs). One dummy SCCB write (e.g., write to a non-existing address) needs to be performed after the real SCCB write, in order to get the correct CRC result. CRC registers appear as part of embedded data (without being reset automatically).

table 5-14 SCCB CRC registers

address	register name	default value	R/W	description
0x7FF6	SCCB_CRC_H	–	R	SCCB CRC High Byte
0x7FF7	SCCB_CRC_L	–	R	SCCB CRC Low Byte

6 SCCB interface

The SCCB interface controls the image sensor operation.

6.1 SCCB timing

figure 6-1 SCCB interface timing

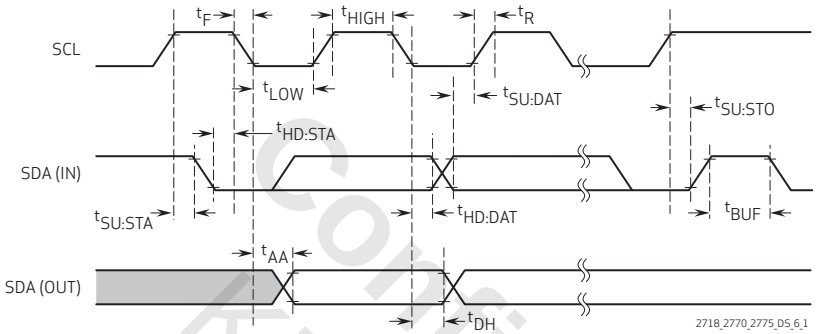


table 6-1 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			1000[c]	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz mode

b. timing measurement shown at the beginning of the rising edge or the end of the falling edge signifies 30%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the end of rising edge or the beginning of the falling edge signifies 70%

c. For 1000 kHz mode, minimum input clock is 10 MHz. For 400 kHz or less mode, minimum input clock is 6 MHz.

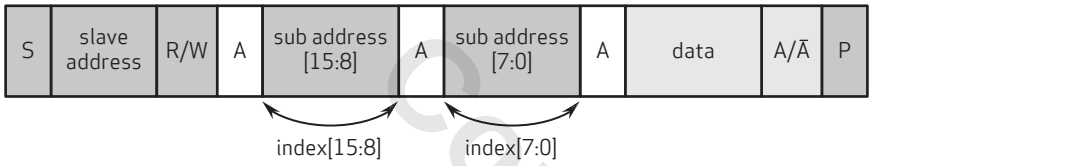
6.2 direct access mode

6.2.1 message format

The OV2718 supports the message format shown in **figure 6-2**. The repeated START (Sr) condition is shown in **figure 6-3** and **figure 6-5**.

figure 6-2 message type

message type: 16-bit sub-address, 8-bit data, and 7-bit slave address



from slave to master
from master to slave
direction depends on operation

S START condition
P STOP condition
Sr repeated START condition

A acknowledge
Ā negative acknowledge

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6.2.2 read / write operation

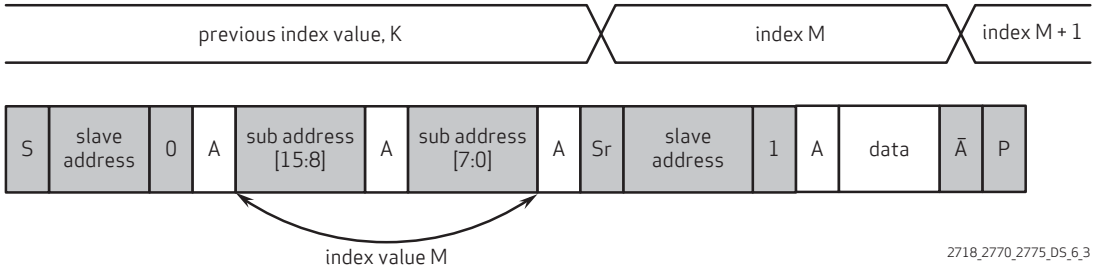
The OV2718 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

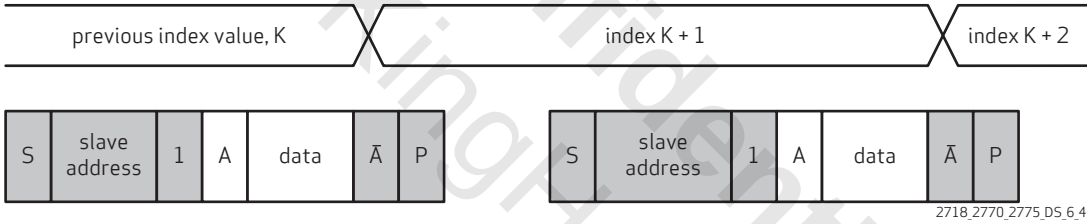
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 6-3**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-3 SCCB single read from random location



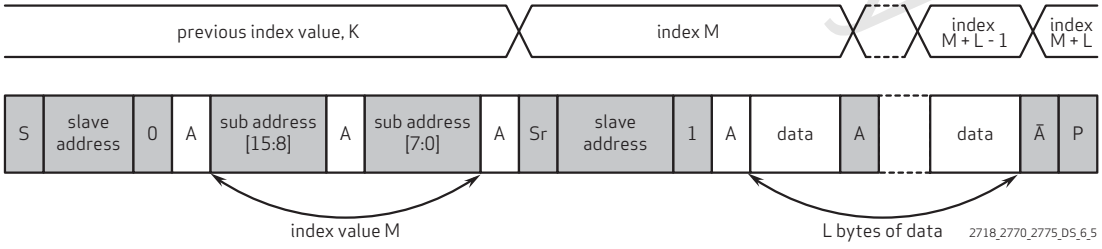
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 6-4**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-4 SCCB single read from current location



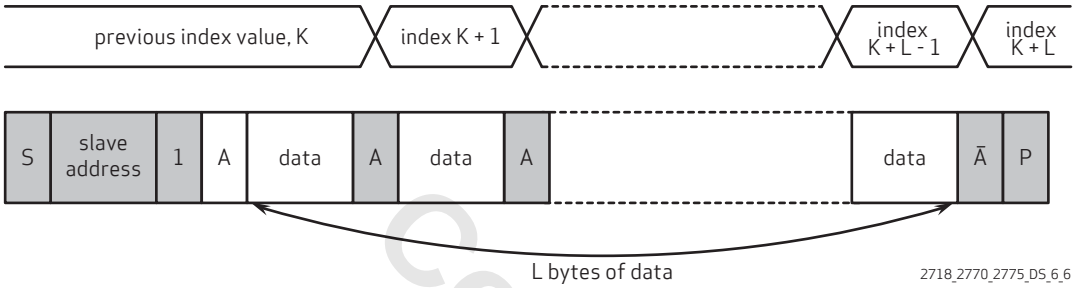
The sequential read from a random location is illustrated in **figure 6-5**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 6-5 SCCB sequential read from random location



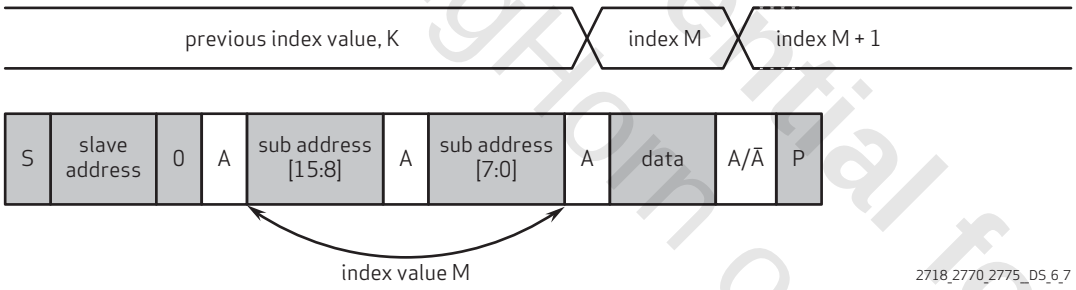
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation. as shown in **figure 6-6**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-6 SCCB sequential read from current location



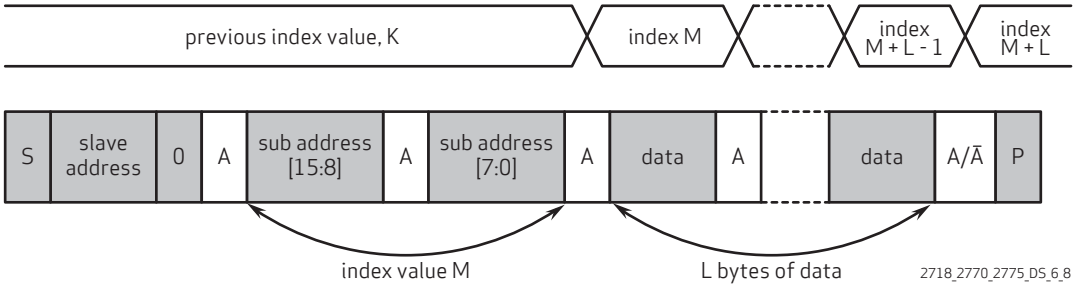
The write operation to a random location is illustrated in **figure 6-7**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 6-7 SCCB single write to random location



The sequential write is illustrated in **figure 6-8**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 6-8 SCCB sequential write to random location



7 OTP memory

The OV2718 has a total of 512 bytes of OTP memory. Using the auto load function, the data in the OTP memory is written to registers when sensor is powered up, e.g. temperature calibration data.

7.1 OTP memory map

The OTP usage is designed to be as shown in **table 7-1**:

table 7-1 OTP memory map overview

start address	end address	bytes usage	assignment
0x7A00	0x7A0F	16	wafer info
0x7A10	0x7BFF	–	reserved

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-50°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +85°C sensor junction temperature
stable image temperature[b]	0°C to +60°C junction temperature

a. sensor functions in the operating range; however, some image quality changes may be noticed at the temperature extremes

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max	unit
supply					
$V_{DD-3.3}$	supply voltage (analog)	3.14	3.3	3.47	V
$V_{DD-1.3}$	supply voltage (digital circuit)	1.2	1.3	1.4	V
$V_{DD-1.8}$	supply voltage (digital I/O + AVDD)	1.7	1.8	1.9	V
$I_{DD-3.3}$	active (operating) current			20	mA
$I_{DD-1.3}$				227	mA
$I_{DD-1.8}$				17	mA
$I_{DDS-PWDN-3.3}$[a]	standby current[b]			3	µA
$I_{DDS-PWDN-1.3}$				1	µA
$I_{DDS-PWDN-1.8}$				4	µA
digital inputs (typical conditions: AVDD18 =1.8V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[c]	SCL and SDA	-0.5	0	0.54	V
V_{IH}[c]	SCL and SDA	1.26	1.8	2.3	V

a. standby current without input clock

b. standby current based on room temperature

c. based on DOVDD = 1.8V.

8.4 AC characteristics

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	36	MHz
t_r, t_f	clock input rise/fall time			5	ns

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

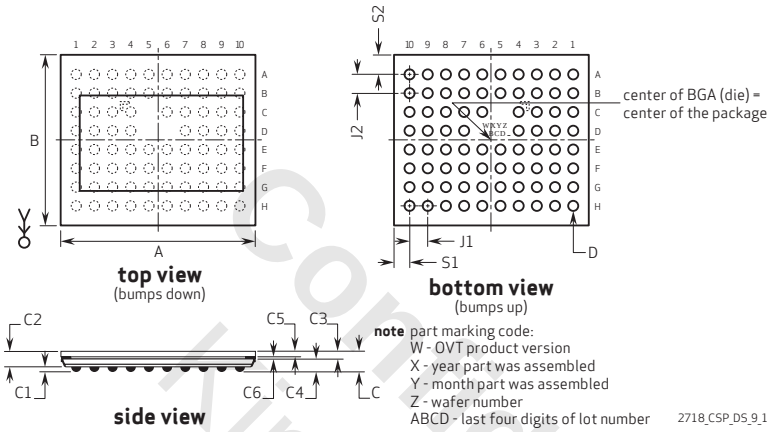
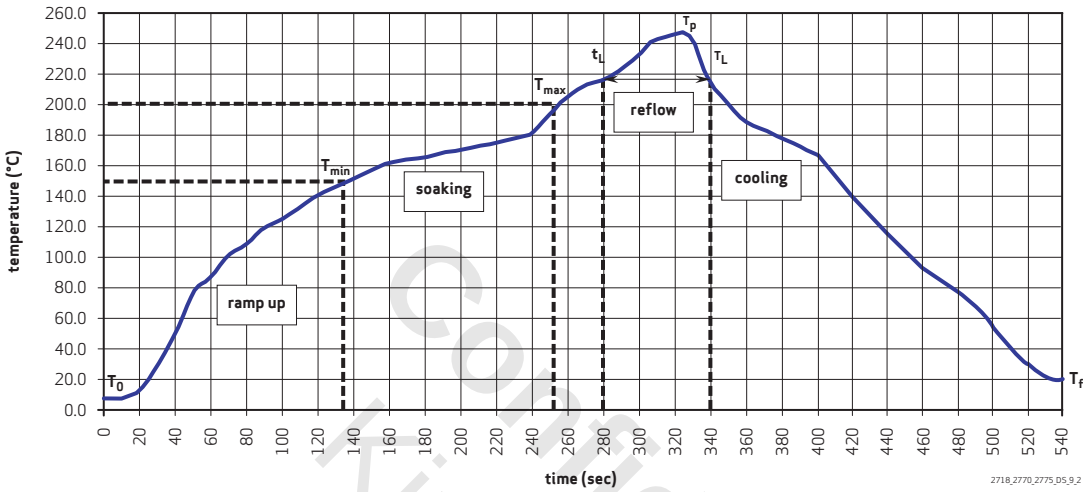


table 9-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	6509	6534	6559	µm
package body dimension y	B	5699	5724	5749	µm
package height	C	845	922.5	1000	µm
ball height	C1	300	337.5	375	µm
package body thickness	C2	515	580	645	µm
thickness of glass surface to wafer	C3	425	445	465	µm
image plane height	C4	405	472.5	540	µm
glass thickness	C5	385	400	415	µm
air gap between die and glass	C6	40	45	50	µm
ball diameter	D	385	417.5	450	µm
total pin count	N		77 (25 NC)		
pins pitch x-axis	J1		610		µm
pins pitch y-axis	J2		630		µm
edge-to-pin center distance along x	S1	492	522	552	µm
edge-to-pin center distance along y	S2	627	657	687	µm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note

The OV2718 uses a lead free package.

table 9-2 reflow conditions[ab]

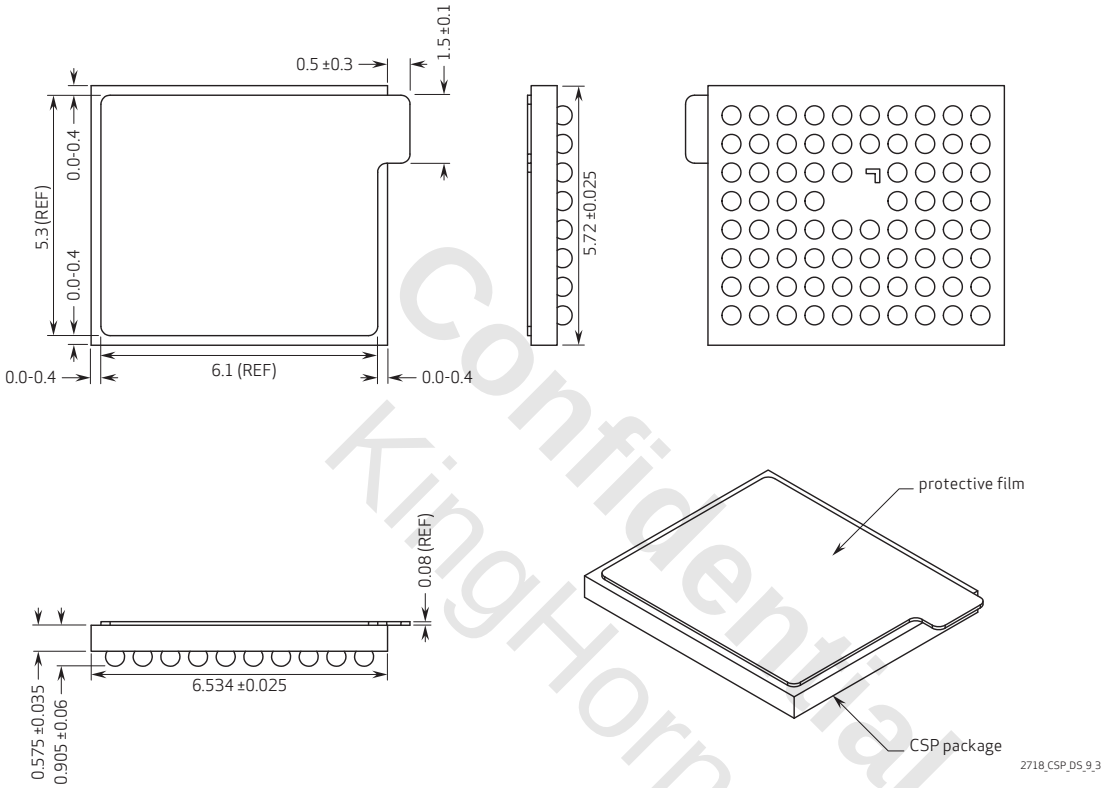
zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5°C (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_P to T_L)	cooling from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM<500 as recommendation

9.3 protective film specifications

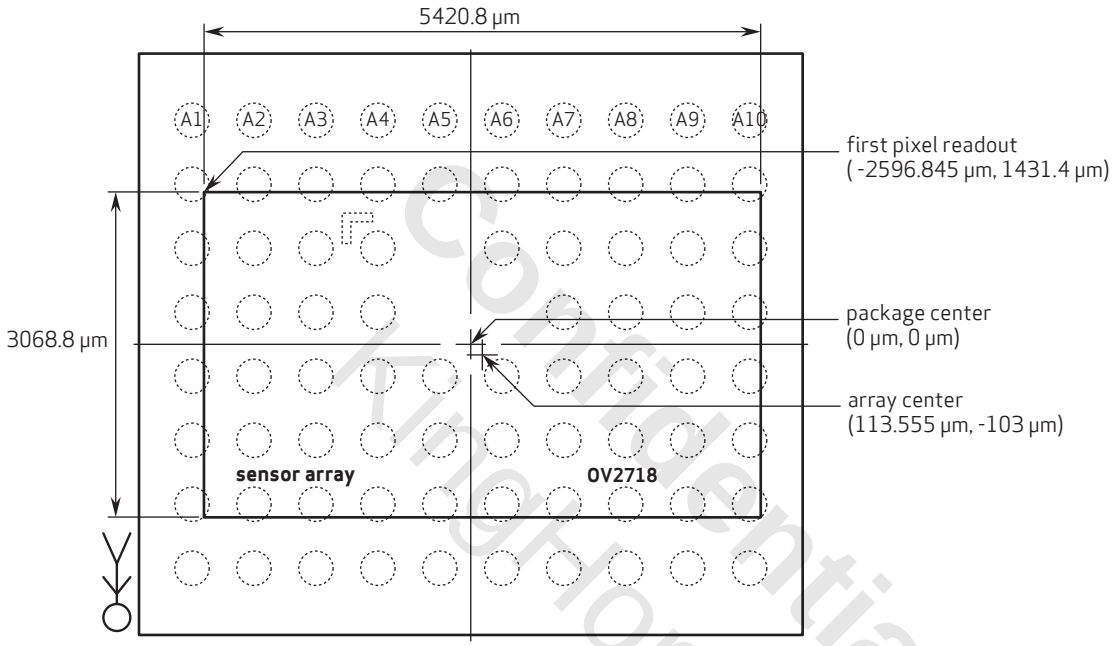
figure 9-3 protective film specifications



10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 oriented down on the PCB.

2718_CSP_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

table 10-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.00
0.10	0.311	0.90
0.20	0.623	1.80
0.30	0.934	2.70
0.40	1.246	3.60
0.50	1.557	4.50
0.60	1.868	5.40
0.70	2.180	6.30
0.80	2.491	7.20
0.90	2.803	8.10
1.00	3.114	9.00

appendix A register table

A.1 module name and address range

table A-1 module name and address range

module name	address range
DIGITAL CORE	0x3000~0x301B
ANALOG CONTROL	0x303A~0x3050
ASIL CONTROL	0x3080~0x3094
OUTPUT TIMING CONTROL	0x30A0~0x310E
BLC CONTROL	0x3140~0x3184
FORMAT CONTROL	0x3190~0x31A7
DVP CONTROL	0x31B0~0x31BA
MIPI CONTROL	0x31D0~0x321B
LVDS CONTROL	0x3230~0x323D
ISP CONTROL	0x3250~0x3258
DCG CONTROL	0x3270~0x327F
LENC CONTROL	0x3330~0x334E
AWB GAIN CONTROL	0x3360~0x339B
OTP DPC CONTROL	0x33B0~0x33CB
DPC CONTROL	0x33F5~0x3433
WINDOW CONTROL	0x3440~0x344C
GROUP HOLD CONTROL	0x3460~0x346D
IO CONTROL	0x3480~0x348F
OTP CONTROL	0x34A0~0x34B6
OTP SRAM	0x7A00~0x7BFF
SCCB CONTROL	0x7FF0~0x7FF7

A.2 device control registers

table A-2 provides a description of the device control registers contained in the OV2718. The 7-bit SCCB slave device address is defined by voltage level of GPIO1 at power up: "6C" by default or defined by 0x300C when GPIO1 has a pull-down resistor; "20" when GPIO1 has a pull-up resistor, which is hard coded and cannot be changed.

table A-2 sensor control registers (sheet 1 of 42)

address	register name	default value	R/W	description
0x3000	SCLK_PLL_PRE	0x05	RW	SCLK PLL Pre Divider
0x3001	SCLK_PLL_MULT	0x63	RW	SCLK PLL Multiplier
0x3002	SCLK_PLL_POST	0x03	RW	SCLK PLL Post Divider (1~16)
0x3003	SCLK_PLL_CONFIG	0x01	RW	Bit[7:6]: lock_precision Lock detector precision resolution setting Bit[5:4]: lock_cntref Lock detector counter setting Bit[3]: fastlock_disable 0: Enable fast locking 1: Disable fast locking Bit[2:0]: Cp Charge pump current
0x3004	PCLK_PLL_PRE	0x06	RW	PCLK PLL Pre Divider
0x3005	PCLK_PLL_PDIV	0x7B	RW	PCLK PLL Div 1 (1~256)
0x3006	PCLK_PLL_SDIV	0x00	RW	PCLK PLL Div 2
0x3007	PCLK_PLL_POST	0x07	RW	PCLK PLL Post Divider (1~16)
0x3008	PCLK_PLL_CTRL1	0x01	RW	Bit[7:2]: Not used Bit[1]: pclk_pll_mipi_div Divide frequency to MIPI/LVDS by 2 Bit[0]: pclk_pll_enable Enable PLL1
0x3009	PCLK_PLL_CTRL2	0x00	RW	Bit[7]: Not used Bit[6:5]: ssc_cntstep Select SSC counter step number Bit[4:2]: ssc_cntck Set SSC counter frequency Bit[1]: ssc_en Enable SSC mode Bit[0]: frac_en Enable fractional mode
0x300A	CHIP_ID_H	0x27	R	Chip ID
0x300B	CHIP_ID_L	0x70	R	Chip ID

table A-2 sensor control registers (sheet 2 of 42)

address	register name	default value	R/W	description
0x300C	SCCB_ID	0x6C	RW	Bit[7:1]: sccb_id_n Bit[0]: sccb_id_sel
0x300D	SUB_ID	0xF0	RW	Chip Subversion ID, Set by ROM loader
0x3010	MAN_ID_H	–	R	Manufacturer ID High Byte
0x3011	MAN_ID_L	–	R	Manufacturer ID Low Byte
0x3012	SFW_CTRL1	0x00	RW	Software Control 1 Bit[7:1]: Not used Bit[0]: sfw_stb 0: Software standby 1: Streaming
0x3013	SFW_CTRL2	0x00	RW	Bit[7:1]: Not used Bit[0]: sfw_rst Software reset
0x3014	PWUP_CTRL	0x04	RW	Bit[7]: sel_src 0: Selects SCLK PLL 1: Selects PLCK PLL as the source for SCLK Bit[6]: sel_phase 1: Inverts the phase of selected clock for SCLK Bit[5]: wdp_rom_crc_en Enable for triggering watchdog pulse if ROM loader CRC fails Bit[4]: wdp_pll_lock_en Enable for triggering watchdog pulse if PLLs are not locked Bit[3]: lock_pll_settings Locks all the registers from sclk_pll_pre to pclk_pll_ctrl2 Bit[2]: use_pll_lock 0: Old method PLL lock 1: Use PLL lock from PLLs Bit[1]: early_pll 0: Turn PLL off in SW_STANDBY 1: Turn PLL on in SW_STANDBY Bit[0]: early_ana 0: Turn analog off in SW_STANDBY 1: Turn analog on in SW_STANDBY
0x3015	NOT USED	–	–	Not Used

table A-2 sensor control registers (sheet 3 of 42)

address	register name	default value	R/W	description
0x3016	POST	–	R	Bit[7:6]: Not used Bit[5:2]: sc_state Bit[1]: Not used Bit[0]: romloader_ok
0x3017	PCLK_PLL_DSM_MAX_H	0x00	RW	PCLK PLL Fractional Div[19:18] (SSC Maximum High Byte)
0x3018	PCLK_PLL_DSM_MAX_L	0x00	RW	PCLK PLL Fractional Div[17:10] (SSC Maximum Low Byte)
0x3019	PCLK_PLL_DSM_MIN_H	0x00	RW	PCLK PLL Fractional Div[9:8] (SSC Minimum High Byte)
0x301A	PCLK_PLL_DSM_MIN_L	0x00	RW	PCLK PLL Fractional Div[7:0] (SSC Minimum Low Byte)
0x301B	PCLK_PLL_CONFIG	0x01	RW	Bit[7:6]: lock_precision Lock detector precision resolution setting Bit[5:4]: lock_cntref Lock detector counter setting Bit[3]: fastlock_disable 0: Enable fast locking 1: Disable fast locking Bit[2:0]: Cp Charge pump current
0x303A	ANA_CB	0x04	RW	Bit[7:6]: Not used Bit[5]: cb_en Enable color bars Bit[4]: cb_mode 0: Do not swap color bars mid-array 1: Swap color bars mid-array (mirror rows) Bit[3]: cb_swap 0: Do not swap color bars 1: Swap color bars (mirror columns) Bit[2:0]: cb_adjust LCB current level (color bar intensity)
0x3080	WIN_ST_H	0x00	RW	High Byte Start Window Column Address
0x3081	WIN_ST_L	0x00	RW	Low Byte Start Window Column Address
0x3082	WIN_END_H	0x01	RW	High Byte End Window Column Address
0x3083	WIN_END_L	0xE3	RW	Low Byte End Window Column Address

table A-2 sensor control registers (sheet 4 of 42)

address	register name	default value	R/W	description
0x3084	ASIL_CTRL	0x05	RW	Bit[7]: asil_data_en Bit[6]: Not used Bit[5]: asil_en_dark Enables ASIL for dark rows Bit[4]: asil_en Enables ASIL (analog and logic) Bit[3:0]: asil_pattern Defines which columns (even or odd) are high and low
0x3085	ASIL_CTRL2	0x00	RW	Bit[7:4]: Not used Bit[3]: asil_on_hcg Bit[2]: asil_row_delay Delay selected ASIL row pointer by 1 row Bit[1:0]: asil_again ASIL analog gain
0x3086	DELTA_HIGH	0x10	RW	Defines the Acceptance Range for Measured High Value
0x3087	DELTA_LOW	0x10	RW	Defines the Acceptance Range for Measured Low Value
0x3089	N_POINTER_H	0x00	RW	A Pointer to the Fail to Be Shown, High Byte
0x308A	N_POINTER_L	0x01	RW	A Pointer to the Fail to Be Shown, Low Byte
0x308B	ROW_NR_H	–	R	High Bits for the Row Number for the Nth Fail
0x308C	ROW_NR_L	–	R	Low Byte for the Row Number for the Nth Fail
0x308D	COL_NR_H	–	R	High Bits for the Col Number for the Nth Fail
0x308E	COL_NR_L	–	R	Low Byte for the Col Number for the Nth Fail
0x308F	FAILED_NR_H	–	R	Number of Failed Positions, High Byte
0x3090	FAILED_NR_L	–	R	Number of Failed Positions, Low Byte
0x3091	HIGH_LEVEL	–	R	Measured Level on High ASIL Signal
0x3092	LOW_LEVEL	–	R	Measured Level on Low ASIL Signal
0x3093	FAILED_NR_THRE_H	0x00	RW	Failed NR Threshold to Trigger Watchdog Pulse, High Byte. Disabled if Set to 0xFFFF
0x3094	FAILED_NR_THRE_L	0x00	RW	Failed NR Threshold to Trigger Watchdog Pulse, Low Byte. Disabled if Set to 0xFFFF
0x30A0	CROP_H_ST_H	0x00	RW	Start Address Horizontal High Byte
0x30A1	CROP_H_ST_L	0x00	RW	Start Address Horizontal Low Byte
0x30A2	CROP_V_ST_H	0x00	RW	Start Address Vertical High Byte

table A-2 sensor control registers (sheet 5 of 42)

address	register name	default value	R/W	description
0x30A3	CROP_V_ST_L	0x00	RW	Start Address Vertical Low Byte
0x30A4	CROP_H_END_H	0x07	RW	End Address Horizontal High Byte
0x30A5	CROP_H_END_L	0x8F	RW	End Address Horizontal Low Byte
0x30A6	CROP_V_END_H	0x04	RW	End Address Vertical High Byte
0x30A7	CROP_V_END_L	0x47	RW	End Address Vertical Low Byte
0x30A8	ODP_H_OFFS_H	0x00	RW	Output Data Path Horizontal Offs High Byte
0x30A9	ODP_H_OFFS_L	0x00	RW	Output Data Path Horizontal Offs Low Byte
0x30AA	ODP_V_OFFS_H	0x00	RW	Output Data Path Vertical Offs High Byte
0x30AB	ODP_V_OFFS_L	0x00	RW	Output Data Path Vertical Offs Low Byte
0x30AC	ODP_H_SIZE_H	0x07	RW	Output Data Path Horizontal Size High Byte
0x30AD	ODP_H_SIZE_L	0x90	RW	Output Data Path Horizontal Size Low Byte
0x30AE	ODP_V_SIZE_H	0x04	RW	Output Data Path Vertical Size High Byte
0x30AF	ODP_V_SIZE_L	0x4A	RW	Output Data Path Vertical Size Low Byte
0x30B0	HTS_H	0x09	RW	Line Length High Byte
0x30B1	HTS_L	0x98	RW	Line Length Low Byte
0x30B2	VTS_H	0x04	RW	Frame Length High Byte
0x30B3	VTS_L	0x65	RW	Frame Length Low Byte
0x30B4	EXTRA_DELAY_H	0x00	RW	(fs_delay) the Last Row Can Be Extended by This Number of Clocks. Reset by sensor_ctrl.extra_ctrl
0x30B5	EXTRA_DELAY_L	0x00	RW	(fs_delay) the Last Row Can Be Extended by This Number of Clocks. Reset by sensor_ctrl.extra_ctrl
0x30B6	CEXP_DCG_H	0x00	RW	Frame DCG (HCG/LCG) Exposure Time (Coarse/in Rows) High Byte
0x30B7	CEXP_DCG_L	0x10	RW	Frame DCG (HCG/LCG) Exposure Time (Coarse/in Rows) Low Byte

table A-2 sensor control registers (sheet 6 of 42)

address	register name	default value	R/W	description
0x30BB	CG_AGAIN	0x00	RW	Bit[7]: Not used Bit[6]: cg_lin Linear conversion gain Bit[5:4]: Not used Bit[3:2]: again_lcg LCG analog gain Bit[1:0]: again_hcg HCG/linear analog gain
0x30BC	EXTRA_VTS	0x00	RW	Delay Added to VTS. Reset by sensor_ctrl.extra_ctrl
0x30BD	SENSOR_CTRL	0x03	RW	Bit[7]: Not used Bit[6]: fsin_intr_en When high, external input can generate interrupt when FSIN arrives Bit[5]: fsin_retro_mode When high, makes FSIN logic work Bit[4]: fsin_en When high, FSIN mode is enabled Bit[3]: low_power_mode When high, sensor will not read the exposures that are disabled (single or 2 expo) Bit[2:1]: Not used Bit[0]: extra_ctrl When high, extra delays will be reset when used once
0x30BE	ROW_ADDR_CTRL	0x5C	RW	Bit[7:6]: Not used Bit[5:0]: row_first_active Array row address of first active row
0x30BF	SKIP_CTRL	0x00	RW	Bit[7:3]: Not used Bit[2]: Monochrome Monochrome readout mode Bit[1]: Vsub2 Skip 2/2 rows or 1/1 rows in monochrome Bit[0]: Hsub2 Skip 2/2 columns or 1/1 columns in monochrome
0x30C0	READ_MODE	0x10	RW	Bit[7:4]: Not used Bit[3]: Flip Bit[2]: Mirror Bit[1:0]: Not used

table A-2 sensor control registers (sheet 7 of 42)

address	register name	default value	R/W	description
0x30C1	READ_CTRL	0x04	RW	Bit[7:3]: Not used Bit[2]: show_emb_rows Show embedded rows Bit[1:0]: Not used
0x30C5	ALU_TEST_CTRL	0x00	RW	Bit[7:2]: Not used Bit[1]: alu_mbist_mode Bit[0]: Reserved
0x30C7	TC_R_RST_NUM_H	0x00	RW	tc_r_rst_num High Byte
0x30C8	TC_R_RST_NUM_L	0x00	RW	tc_r_rst_num Low Byte
0x30C9	EXP_DCG_H	–	R	Frame DCG (HCG/LCG) Exposure Time (in Rows) High Byte
0x30CA	EXP_DCG_L	–	R	Frame DCG (HCG/LCG) Exposure Time (in Rows) Low Byte
0x30D0	CG_AGAIN_USE	–	R	Bit[7]: Not used Bit[6]: cg_lin Linear cg Bit[5:4]: Not used Bit[3:2]: again_lcg LCG again 2'bXX Bit[1:0]: again_l HCG again 2'bXX
0x30D1	ASIL_PATTERN_CTRL	0x04	RW	Bit[7:2]: Not used Bit[1]: pattern_en Enable pattern Bit[0]: pulse_en Enable pulsation of pattern
0x30D2	ASIL_PATTERN_LOW	0x00	RW	Low Pixel Value in ASIL Pattern
0x30D3	ASIL_PATTERN_HIGH	0x80	RW	High Pixel Value in ASIL Pattern
0x30D4	COL_TAG_CTRL	0x00	RW	Bit[7:4]: col_tag_width Column tagger width Bit[3:2]: Not used Bit[1]: col_tag_inv Invert column tagger Bit[0]: col_tag_en Enable column tagger
0x30D5	FCNT_3	–	R	Frame Count Byte 3
0x30D6	FCNT_2	–	R	Frame Count Byte 2
0x30D7	FCNT_1	–	R	Frame Count Byte 1
0x30D8	FCNT_0	–	R	Frame Count Byte 0

table A-2 sensor control registers (sheet 8 of 42)

address	register name	default value	R/W	description
0x30D9	PRE_PRECHARGE	0x08	RW	Bit[7:6]: Not used Bit[5:2]: pre_precharge_rows Number of rows ahead of precharge Bit[1]: Reserved Bit[0]: pre_precharge_en_l
0x30DA	PRE_PRECHARGE_ THRES	0x64	RW	When DCG Exposure Is Larger Than Threshold, Pre-precharge Is Disabled
0x30E4	VFPN_READ_CTRL	0x64	RW	Bit[7]: Not used Bit[6]: vfpn_on_dummy_btm VFPN rows on 'vfpn_rows' rows at bottom of active array Bit[5]: vfpn_on_dummy_top VFPN rows on 'vfpn_rows' rows at top of active array Bit[4]: read_vfpn_rows Enable output of 'vfpn_rows+1' dedicated VFPN rows at end of frame Bit[3:0]: vfpn_rows Number of VFPN rows
0x30FF	SEQ_CRC_H	–	R	Sequencer CRC from Last Row High Byte
0x3100	SEQ_CRC_L	–	R	Sequencer CRC from Last Row Low Byte
0x3101	SEQ_CRC_EXPECT_H	0x00	RW	Expected Sequencer CRC High Byte
0x3102	SEQ_CRC_EXPECT_L	0x00	RW	Expected Sequencer CRC Low Byte
0x3103	SEQ_STATUS	0x00	RW	Bit[7:4]: Not used Bit[3]: wdp_crc_en Enables seq_crc_fail to contribute to watch dog pulse generation Bit[2]: wdp_timing_en Enables seq_timing_fail to contribute to watch dog pulse generation Bit[1]: seq_crc_fail Status bit is set to one if sequencer CRC does not match (write 0 to reset) Bit[0]: seq_timing_fail Status bit is set to one if sequencer did not finish within HTS

table A-2 sensor control registers (sheet 9 of 42)

address	register name	default value	R/W	description
0x310E	LOCK_TC	0x00	RW	Bit[7:5]: Not used Bit[4]: lock_read_mode Bit[3]: lock_vts Bit[2]: lock_hts Bit[1]: lock_h_crop Bit[0]: lock_v_crop
0x3140	BLC_CTRL	0x02	RW	Bit[7:4]: Not used Bit[3]: blc_cont_update_mode Enable BLC recalculation on every frame Bit[2]: Not used Bit[1]: blc_dither_en Enable dithering on unused sub-LSBS of incoming data Bit[0]: show_dark_rows Show the dark rows in the image
0x3141	BLC_SMOOTHING	0x07	RW	Filter Coefficient Alpha = (Smoothing+1)/32 If Zero, New Value Is Not Used.
0x3142	D_VALUE_HCG	0x00	RW	Signed Fractional (/256) Value Between -128/256 and 128/256 to Adjust DL'=DL(1+D) for HCG Exposure
0x3143	D_VALUE_LCG	0x00	RW	Signed Fractional (/256) Value Between -128/256 and 128/256 to Adjust DL'=DL(1+D) for LCG Exposure
0x3145	K_OFFSET_HCG	0x00	RW	Signed Offset to Adjust DL' = DL + K × again/16 for HCG Exposure
0x3146	K_OFFSET_LCG	0x00	RW	Signed Offset to Adjust DL' = DL + K × again/16 for LCG Exposure
0x3148	BLC_OVERRIDE_HCG_H	0x00	RW	Manual BLC Override Value for HCG Exposure, MSB
0x3149	BLC_OVERRIDE_HCG_L	0x00	RW	Manual BLC Override Value for HCG Exposure, LSB
0x314A	BLC_OVERRIDE_LCG_H	0x00	RW	Manual BLC Override Value for LCG Exposure, MSB
0x314B	BLC_OVERRIDE_LCG_L	0x00	RW	Manual BLC Override Value for LCG Exposure, LSB

table A-2 sensor control registers (sheet 10 of 42)

address	register name	default value	R/W	description
0x314E	BLC_TRIGGER	0x1C	RW	Bit[7:5]: Not used Bit[4]: blc_exp_changed_trig_en Enable triggering of BLC after exposure changes Bit[3]: blc_gain_changed_trig_en Enable triggering of BLC after gain changes Bit[2]: blc_restart_frame_trig_en Enable triggering of BLC at restart Bit[1]: blc_hard_trigger_en Enable hard triggering for manual, threshold crossed, and continuos update triggers as well Bit[0]: blc_manual_trig Transition 0->1 causes trigger. Must be reset by user.
0x314F	BLC_TRIGGER_ THRE_HCG	0x10	RW	Threshold for Triggering of BLC for HCG Exposure (no sub-LSBS). 0xFF Will Turn Threshold Triggering Off. Difference Between Dark Level for Current Frame and Applied Correction Is Compared to the Threshold.
0x3150	BLC_TRIGGER_ THRE_LCG	0x10	RW	Threshold for Triggering of BLC for LCG Exposure (no sub-LSBS). 0xFF Will Turn Threshold Triggering Off. Difference Between Dark Level for Current Frame and Applied Correction Is Compared to the Threshold.
0x3152	BLC_TRIGGER_ THRE_HARD_HCG	0x80	RW	Threshold for Hard Triggering of BLC for HCG Exposure (no sub-LSBS). 0xFF Will Turn Hard Threshold Triggering Off. Difference Between Dark Level for Current Frame and Applied Correction Is Compared to the Threshold.
0x3153	BLC_TRIGGER_ THRE_HARD_LCG	0x80	RW	Threshold for Hard Triggering of BLC for LCG Exposure (no sub-LSBS). 0xFF Will Turn Hard Threshold Triggering Off. Difference Between Dark Level for Current Frame and Applied Correction Is Compared to the Threshold.
0x3155	DITHER_GAIN_ THRESHOLD	0x00	RW	Gain Threshold for Enabling Dither. Compared to Upper 8 Bits of Digital Gain Value (a value of 0 means always enabled)
0x3156	RESTART_FRAMES	0x01	RW	Number of Frames With Continuous Update After Restart (0xFF Is always triggered, 0x00 will give 1 frame)

table A-2 sensor control registers (sheet 11 of 42)

address	register name	default value	R/W	description
0x3157	AB_CTRL	0x00	RW	Controls AB Mode Operation Bit[7:2]: Not used Bit[1]: Bframe Selects between A (0) and B (1) frames Bit[0]: ab_mode Enable AB mode
0x3158	BLC_MAX_CORRECTION_H	0x0F	RW	Maximum Value of BLC Correction, MSB
0x3159	BLC_MAX_CORRECTION_L	0xFF	RW	Maximum Value of BLC Correction, LSB
0x315A	DIG_GAIN_HCG_H	0x01	RW	Digital Gain for HCG, MSB (Format 6.8)
0x315B	DIG_GAIN_HCG_L	0x00	RW	Digital Gain for HCG, LSB
0x315C	DIG_GAIN_LCG_H	0x01	RW	Digital Gain for LCG, MSB (Format 6.8)
0x315D	DIG_GAIN_LCG_L	0x00	RW	Digital Gain for LCG, LSB
0x3160	BLC_TARGET_HCG_H	0x00	RW	Black Level Target HCG Exposure High Byte
0x3161	BLC_TARGET_HCG_L	0x20	RW	Black Level Target HCG Exposure Low Byte
0x3162	BLC_TARGET_LCG_H	0x00	RW	Black Level Target LCG Exposure High Byte
0x3163	BLC_TARGET_LCG_L	0x20	RW	Black Level Target LCG Exposure Low Byte
0x3166	DIG_GAIN_FS2_HCG_H	–	R	Read Back of Frame Synchronized Digital Gain for HCG Exposure, MSB
0x3167	DIG_GAIN_FS2_HCG_L	–	R	Read Back of Frame Synchronized Digital Gain for HCG Exposure, LSB
0x3168	DIG_GAIN_FS2_LCG_H	–	R	Read Back of Frame Synchronized Digital Gain for LCG Exposure, MSB
0x3169	DIG_GAIN_FS2_LCG_L	–	R	Read Back of Frame Synchronized Digital Gain for LCG Exposure, LSB
0x316A	DIG_GAIN_FS2_HCG_H	–	R	Read Back of Frame Synchronized Digital Gain for HCG Exposure, MSB
0x316C	BLC_TARGET_FS2_HCG_H	–	R	Read Back of Black Level Target HCG Exposure High Byte
0x316D	BLC_TARGET_FS2_HCG_L	–	R	Read Back of Black Level Target HCG Exposure Low Byte
0x316E	BLC_TARGET_FS2_LCG_H	–	R	Read Back of Black Level Target LCG Exposure High Byte

table A-2 sensor control registers (sheet 12 of 42)

address	register name	default value	R/W	description
0x316F	BLC_TARGET_FS2_LCG_L	–	R	Read Back of Black Level Target LCG Exposure Low Byte
0x3172	DARK_CURRENT_HCG_H	–	R	Dark Current Compensation for HCG, MSB (Signed)
0x3173	DARK_CURRENT_HCG_L	–	R	Dark Current Compensation for HCG, LSB (3 Sub-LSBs)
0x3174	DARK_CURRENT_LCG_H	–	R	Dark Current Compensation for LCG, MSB (Signed)
0x3175	DARK_CURRENT_LCG_L	–	R	Dark Current Compensation for LCG, LSB (3 sub-LSBs)
0x3178	ROW_AVERAGE_HCG_H	–	R	Row Average (Accumulator Value) for HCG, MSB (Signed)
0x3179	ROW_AVERAGE_HCG_L	–	R	Row Average (Accumulator Value) for HCG, LSB (3 Sub-LSBs)
0x317A	ROW_AVERAGE_LCG_H	–	R	Row Average (Accumulator Value) for LCG, MSB (Signed)
0x317B	ROW_AVERAGE_LCG_L	–	R	Row Average (Accumulator Value) for LCG, LSB (3 Sub-LSBs)
0x317E	D_VALUE_FS2_HCG	–	R	Read Back of Frame Synchronized d_value for HCG
0x317F	D_VALUE_FS2_LCG	–	R	Read Back of Frame Synchronized d_value for LCG
0x3181	K_OFFSET_FS2_HCG	–	R	Read Back of Frame Synchronized k_offset for HCG
0x3182	K_OFFSET_FS2_LCG	–	R	Read Back of Frame Synchronized k_offset for LCG
0x3184	BFRAME_FS2	–	R	Read Back of Frame Synchronized Bframe Bit from ab_ctrl Register

table A-2 sensor control registers (sheet 13 of 42)

address	register name	default value	R/W	description
0x3190	INTERFACE_CTRL0	0x07	RW	Bit[7]: channel_cfg Channel configuration Bit[6:5]: Reserved Bit[4]: no_comp When high, single 12-bit data are sent without compression Bit[3]: lin_enable Linear mode enable Bit[2]: Reserved Bit[1:0]: data_width 00: Not used 01: 2x12 10: Comb 12 11: Comb 16
0x3191	INTERFACE_CTRL1	0x99	RW	Bit[7]: img_size_vfifo_sel Select automatically calculated image size Bit[6]: Not used Bit[5]: hts_pclk_man_en HTS PCLK manual override when the SCLK to PCLK Bit[4]: discard_fake_ro Do not output fake data Bit[3]: vfifo_fake_ro Emulate VFIFO read-out in unalign MIPI-mode Bit[2]: Not usedlvds_16bit_markers LVDS generate 16-bit markers instead of 8-bit Bit[1:0]: if_mode 00: DVP 01: MIPI 10: LVDS 11: Not used
0x3193	HTS_PCLK_MAN_H	0x08	RW	HTS in PCLKs, Manual Override Value High Byte (DVP Only)
0x3194	HTS_PCLK_MAN_L	0x13	RW	HTS in PCLKs, Manual Override Value Low Byte (DVP Only)
0x3195	VFIFO_READ_LEVEL	0x33	RW	vfifo_read_level

table A-2 sensor control registers (sheet 14 of 42)

address	register name	default value	R/W	description
0x31A0	MIPI_FORMAT	0x2C	RW	Bit[7]: mipi_byte_switch MIPI byte switch in 16-bit mode Bit[6]: Not used Bit[5:4]: mipi_vch_id_third Virtual channel ID for third channel, only used in 3-exposure mode Bit[3:2]: mipi_vch_id_sec Virtual channel ID for secondary channel, not used in linear mode Bit[1:0]: mipi_vch_id_main Virtual channel ID for main channel
0x31A1	MIPI_DUMMY_DATA	0x55	RW	Dummy Data to Output During Dummy Rows (MSB-Aligned to 12-bit)
0x31A2	FORMAT_SETTINGS	0x00	RW	Bit[7:6]: Not used Bit[5]: disable_arbiter Disable arbiter (always give VFIFO access to FI1) Bit[4:3]: dvp_16b_opt 00: Advanced 16-bit DVP packing 01: Not used 10: 2-cycle packing option A (MSB) 11: 2-cycle packing option B (12-bit) Bit[2]: reset_crc_error_cnt Write to reset CRC error count Bit[1:0]: flag_2x12 Manual flag settings for 2x12 mode
0x31A3	VFIFO_MANUAL_ OVERRIDE	0x00	RW	Bit[7:6]: vfifo_lane_fill_inc_man Bit[5:4]: vfifo_lane_fill_cap_man Bit[3]: vfifo_lane_fill_man Bit[2:1]: vfifo_inp_data_width_man Bit[0]: vfifo_inp_data_width_man_e
0x31A4	VFIFO_STATUS	–	R	Bit[7:2]: Not used Bit[1]: fo_q_error FO overflow (data is not getting out from VFIFO) Bit[0]: fo_q_empty FO is empty (it should not always be 1)
0x31A5	VFIFO_CRC_ERROR_ COUNT	–	R	VFIFO CRC Error Count, Number of Lines That Failed CRC Check
0x31A6	VFIFO_CRC_ERROR_TH	0x00	RW	VFIFO CRC Error Count Threshold to Trigger Watchdog Pulse. Disabled if '0xFF

table A-2 sensor control registers (sheet 15 of 42)

address	register name	default value	R/W	description
0x31A7	VFIFO_CTRL	0x00	RW	Bit[7:1]: Not used Bit[0]: fo_q_error_wdp_en Enable for triggering watchdog pulse on fo_q_error
0x31B0	VSYNC_WIDTH_LINE_H	0x00	RW	VSYNC Width by Line Number High Byte
0x31B1	VSYNC_WIDTH_LINE_L	0x00	RW	VSYNC Width by Line Number Low Byte
0x31B2	VSYNC_WIDTH_PIXEL_H	0x02	RW	VSYNC Width by Pixel Number High Byte
0x31B3	VSYNC_WIDTH_PIXEL_L	0x00	RW	VSYNC Width by Pixel Number Low Byte, Must Be Larger Than 0
0x31B4	VSYNC_DELAY_H	0x00	RW	VSYNC Delay Count High Byte
0x31B5	VSYNC_DELAY_M	0x01	RW	VSYNC Delay Count Mid Byte
0x31B6	VSYNC_DELAY_L	0x00	RW	VSYNC Delay Count Low Byte
0x31B7	POLARITY_CTRL	0x00	RW	Bit[7]: Reserved Bit[6]: Bit reverse enable Bit[5]: vsync_gate_clk_enable Bit[4]: href_gate_clk_enable Bit[3]: Reserved Bit[2]: href_polarity Bit[1]: vsync_polarity Bit[0]: pclk_polarity Also PCLK gate low enable
0x31B8	BIT_ORDER	0x00	RW	Bit[7:4]: Reserved Bit[3]: bit_test_mode Bit[2]: bit_test_bit10 Bit[1]: bit_test_bit8 Bit[0]: bit_test_enable
0x31B9	BYP_SELECT	0x00	RW	Bit[7:6]: Reserved Bit[5]: data_bit_shift Bit[4]: href_sel Bit[3:0]: bypass_sel
0x31BA	R_FIFO	0x00	RW	Top Sync FIFO Control
0x31D0	CLK_POST_CONST_MIN	0x3C	RW	T(clk_post) Constant Minimum Value, Default Value: 60ns
0x31D1	CLK_POST_UI_MIN	0x34	RW	T(clk_post) UI Minimum Value, Default Value: 52 UIs
0x31D2	CLK_TRAIL_CONST_MIN	0x3C	RW	T(clk_trail) Constant Minimum Value, Default Value: 60ns
0x31D3	CLK_TRAIL_UI_MIN	0x00	RW	T(clk_trail) UI Minimum Value, Default Value: 0 UI

table A-2 sensor control registers (sheet 16 of 42)

address	register name	default value	R/W	description
0x31D4	CLK_PREPARE_CONST_MIN	0x2D	RW	T(clk_prepare) Constant Minimum Value, Default Value: 38 Ns
0x31D5	CLK_PREPARE_UI_MIN	0x00	RW	T(clk_prepare) UI Minimum Value, Default Value: 0 UIs
0x31D6	CLK_ZERO_CONST_MIN1	0x01	RW	T(clk_zero) Constant Minimum Value (High 2 Bits)
0x31D7	CLK_ZERO_CONST_MIN2	0x06	RW	T(clk_zero) Constant Minimum Value, (Low 8 bits) Default Value: 44 Ns
0x31D8	CLK_ZERO_UI_MIN	0x00	RW	T(clk_zero) UI Minimum Value, Default Value: 0 UIs
0x31D9	HS_EXIT_CONST_MIN	0x64	RW	T(hs_exit) Constant Minimum Value, Default Value: 100 Ns
0x31DA	HS_EXIT_UI_MIN	0x00	RW	T(hs_exit) UI Minimum Value, Default Value: 0 UI
0x31DB	HS_PREPARE_CONST_MIN	0x28	RW	T(hs_prepare) Constant Minimum Value, Default Value: 40 Ns
0x31DC	HS_PREPARE_UI_MIN	0x04	RW	T(hs_prepare) UI Minimum Value, Default Value: 4 UI
0x31DD	HS_ZERO_CONST_MIN	0x69	RW	T(hs_zero) Constant Minimum Value, Default Value: 105 Ns
0x31DE	HS_ZERO_UI_MIN	0x0A	RW	T(hs_zero) UI Minimum Value, Default Value: 6 UI
0x31DF	HS_TRAIL_CONST_MIN	0x3C	RW	T(hs_trail) Constant Minimum Value, Default Value: 65 Ns
0x31E0	HS_TRAIL_UI_MIN	0x04	RW	T(hs_trail) UI Minimum Value, Default Value: 4 UI
0x31E1	LPX_CONST_MIN	0x32	RW	T(lpx) Constant Minimum Value, Default Value: 50 Ns
0x31E2	LPX_UI_MIN	0x00	RW	T(lpx) UI Minimum Value, Default Value: 0 UI
0x31E3	MIPI_CLK_PERIOD1	0x00	RW	Clock Period of mipi_clk, Used to Calculate Timing Parameters of MIPI TX (Low 2 Bits, Fraction) Default Value: 2'b00
0x31E4	MIPI_CLK_PERIOD2	0x08	RW	Clock Period of mipi_clk, Used to Calculate Timing Parameters of MIPI TX (High 8 Bits, Integer) 8.00 Ns

table A-2 sensor control registers (sheet 17 of 42)

address	register name	default value	R/W	description
0x31E5	MIPI_LANE_CTRL0	0x92	RW	Bit[7]: ext_timing Finish lane transfer long packet data exactly 0: Not used 1: Do not send any dummy data in data lane. That means trail data will behind the image data i Bit[6]: clk_data_chg Clock lane data change, 2'b01 -> 2'b10 Bit[5]: dis_clk_lane (active high) Disable clock lane Bit[4]: line_sync_en Insert LS/LE in the MIPI TX stream if this bit is set Bit[3]: frame_cnt_zero_c1 MIPI TX channel 1 will keep frame counter zero if this bit is set Bit[2]: frame_cnt_zero_c0 MIPI TX channel 0 will keep frame counter zero if this bit is set Bit[1]: gate_clk_en2 (active high) Gate clock for clock lane when frame blanking time Bit[0]: gate_clk_en1 (active high) Gate clock for clock lane when line/frame blanking time
0x31E6	MIPI_LPKT_MAN	0x00	RW	Bit[7]: Reserved Bit[6]: lpkt_man_en Long packet manual input Bit[5:0]: dt_man Manual data type
0x31E7	MIPI_DI0	0x30	RW	Bit[7:6]: vc_num0 Virtual channel ID for data path 0 Bit[5:0]: img_dt0 Data type for data path 0
0x31E8	MIPI_DI1	0x6C	RW	Bit[7:6]: vc_num1 Virtual channel ID for data path 0 Bit[5:0]: img_dt1 Data type for data path 0
0x31E9	MIPI_DI2	0xAC	RW	Bit[7:6]: vc_num2 Virtual channel ID for data path 0 Bit[5:0]: img_dt2 Data type for data path 0

table A-2 sensor control registers (sheet 18 of 42)

address	register name	default value	R/W	description
0x31EA	MIPI_DI3	0xEC	RW	Bit[7:6]: vc_num3 Virtual channel ID for data path 0 Bit[5:0]: img_dt3 Data type for data path 0
0x31EB	MIPI_EMB	0x7F	RW	Bit[7]: Not used Bit[6]: use_emb_data_type Use embedded data type for embedded data rows Bit[5:0]: emb_dt Data type for embedded data
0x31EC	MIPI_IMG_WIDTHH0	0x0F	RW	Bit[7:0]: img_width[15:8] Channel 0 image width
0x31ED	MIPI_IMG_WIDTHL0	0x20	RW	Bit[7:0]: img_width[7:0] Channel 0 image width
0x31EE	MIPI_IMG_HEIGHTH0	0x04	RW	Bit[7:0]: img_height[15:8] Channel 0 image height
0x31EF	MIPI_IMG_HEIGHTL0	0x48	RW	Bit[7:0]: img_height[7:0] Channel 0 image height
0x31F0	MIPI_IMG_WIDTH1_H	0x07	RW	Bit[7:0]: img_width[15:8] Channel 1 image width
0x31F1	MIPI_IMG_WIDTH1_L	0x90	RW	Bit[7:0]: img_width[7:0] Channel 1 image width
0x31F2	MIPI_IMG_HEIGHTH1	0x04	RW	Bit[7:0]: img_height[15:8] Channel 1 image height
0x31F3	MIPI_IMG_HEIGHT1_L	0x48	RW	Bit[7:0]: img_height[7:0] Channel 1 image height
0x31F4	MIPI_IMG_WIDTH2_H	0x07	RW	Bit[7:0]: img_width[15:8] Channel 2 image width
0x31F5	MIPI_IMG_WIDTH2_L	0x90	RW	Bit[7:0]: img_width[7:0] Channel 2 image width
0x31F6	MIPI_IMG_HEIGHT2_L	0x04	RW	Bit[7:0]: img_height[15:8] Channel 2 image height
0x31F7	MIPI_IMG_HEIGHT2_L	0x48	RW	Bit[7:0]: img_height[7:0] Channel 2 image height
0x31F8	MIPI_IMG_WIDTH3_H	0x07	RW	Bit[7:0]: img_width[15:8] Channel 3 image width
0x31F9	MIPI_IMG_WIDTH3_L	0x90	RW	Bit[7:0]: img_width[7:0] Channel 3 image width

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address	register name	default value	R/W	description
0x31FA	MIPI_IMG_HEIGHT3_H	0x04	RW	Bit[7:0]: img_height[15:8] Channel 3 image height
0x31FB	MIPI_IMG_HEIGHT3_L	0x48	RW	Bit[7:0]: img_height[7:0] Channel 3 image height
0x31FC	MIPI_STATUS	–	R	Bit[7:2]: Not used Bit[1]: mipi_ph_done MIPI has transferred long packet header data. User can modify the data type. Bit[0]: mipi_busy MIPI is transmitting data if this bit is asserted

table A-2 sensor control registers (sheet 20 of 42)

address	register name	default value	R/W	description
0x31FD	MIPI_LANE_CTRL1	0xCB	RW	Bit[7]: hs_zero_sync_en 0: Send 'hs_en' one cycle ahead of hs_zero state 1: Send 'hs_en' sync with hs_zero state Bit[6]: sof_send_fs Send "FS" packet after MIPI received SOF 0: Send "FS" packet when VFIFO data is ready 1: Send "FS" packet when MIPI received SOF Bit[5]: chksum_exchg Long packet checksum byte exchange enable 0: Checksum = CRC[15:0] 1: Checksum = {CRC[7:0], CRC[15:8]} Bit[4]: Reserved Bit[3]: lp_state Low power state when data lane is idle 0: Low power signal for each 1: lp_p or lp_n will stay "1" if the current data lane is not active Bit[2]: pclk_inv_en (active high) PCLK inverse enable (output to PHY) Bit[1]: gen_fe_en1 Force to generate frame end short packet in channel 1 when MIPI TX has transmitted one line if VFIFO of this channel is overflow Bit[0]: gen_fe_en0 Force to generate frame end short packet in channel 0 when MIPI TX has transmitted one line if VFIFO of this channel is overflow

table A-2 sensor control registers (sheet 21 of 42)

address	register name	default value	R/W	description
0x31FE	MIPI_LANE_CTRL2	0x0F	RW	Bit[7]: d4_inv_en Data lane 4 inverse enable Bit[6]: d3_inv_en Data lane 3 inverse enable Bit[5]: d2_inv_en Data lane 2 inverse enable Bit[4]: d1_inv_en Data lane 1 inverse enable Bit[3]: lane4_en Data lane 4 enable Bit[2]: lane3_en Data lane 3 enable Bit[1]: lane2_en Data lane 2 enable Bit[0]: lane1_en Data lane 1 enable
0x31FF	MIPI_LANE_CTRL3	0x03	RW	Bit[7]: ch3_crop_en Channel 3 crop enable 0: Channel 3 crop disable 1: Channel 3 crop enable Bit[6]: ch2_crop_en Channel 2 crop enable 0: Channel 2 crop disable 1: Channel 2 crop enable Bit[5]: ch1_crop_en Channel 1 crop enable 0: Channel 1 crop disable 1: Channel 1 crop enable Bit[4]: ch0_crop_en Channel 0 crop enable 0: Channel 0 crop disable 1: Channel 0 crop enable Bit[3]: fcnt_zero_c3 MIPI TX channel 3 will keep frame counter zero if this bit is set Bit[2]: fcnt_zero_c2 MIPI TX channel 2 will keep frame counter zero if this bit is set Bit[1]: gen_fe_en3 Force to generate frame end short packet in channel 3 when MIPI TX has transmitted one line if VFIFO of this channel is overflow Bit[0]: gen_fe_en2 Force to generate frame end short packet in channel 2 when MIPI TX has transmitted one line if VFIFO of this channel is overflow

table A-2 sensor control registers (sheet 22 of 42)

address	register name	default value	R/W	description
0x3200	MIPI_TST_MODE	0x00	RW	Bit[7:6]: Not used Bit[5]: lp_n_man_data Output manual lower power data in MIPI TX test mode Bit[4]: lp_p_man_data Output manual lower power data in MIPI TX test mode Bit[3]: lp_man_en Output manual low power data enable in low power test mode and de-assert high speed signal (hs_en or valid) Bit[2]: hs_man_en Manual test data will output to PHY when this bit is set and MIPI TX in high speed test mode (reg25 must be set in this case) Bit[1]: tst_mode 0: Test start point sync by "mipi_test" 1: Test start point sync by MIPI RX "prbs_en" Bit[0]: mipi_tst (active high) Test MIPI TX and RX PHY
0x3201	MANUAL_TST_DATA	0xFF	RW	Manual Test Data for MIPI PHY
0x3202	MIPI_TST_CFG	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rx_prbs_en Enable MIPI PHY test including RX PHY and TX PHY
0x3203	MAX_FRAME_CNT0_H	0xFF	RW	High Byte of Maximum Frame Counter of Channel 0
0x3204	MAX_FRAME_CNT0_L	0xFF	RW	Low Byte of Maximum Frame Counter of Channel 0
0x3205	MAX_FRAME_CNT1_H	0xFF	RW	High Byte of Maximum Frame Counter of Channel 1
0x3206	MAX_FRAME_CNT1_L	0xFF	RW	Low Byte of Maximum Frame Counter of Channel 1
0x3207	MAX_FRAME_CNT2_H	0xFF	RW	High Byte of Maximum Frame Counter of Channel 2
0x3208	MAX_FRAME_CNT2_L	0xFF	RW	Low Byte of Maximum Frame Counter of Channel 2
0x3209	MAX_FRAME_CNT3_H	0xFF	RW	High Byte of Maximum Frame Counter of Channel 3

table A-2 sensor control registers (sheet 23 of 42)

address	register name	default value	R/W	description
0x320A	MAX_FRAME_CNT3_L	0xFF	RW	Low Byte of Maximum Frame Counter of Channel 3
0x320E	RAW16	0x30	RW	RAW16 Data Type
0x3210	RAW12	0x2C	RW	RAW12 Data Type
0x3211	RAW10	0x2B	RW	RAW10 Data Type
0x3215	DAT_SEQ_CTRL	0x00	RW	Bit[7:5]: total_seq RGB sequence 000: Sequence = 'BGR' 001: Sequence = 'BRG' 010: Sequence = 'GBR' 011: Sequence = 'GRB' 100: Sequence = 'RGB' Bit[4:3]: high_half_seq Quarter sequence Used to adjust the each 12-bits data sequence 00: data[11:0] 01: {data[9:0],data[11:10]} 10: {data[7:0],data[11:8]} 11: Not used Bit[2]: low_half_seq Low half sequence Used to adjust the low 24-bits data Sequence = 1'b0, data[23:0], = 1'b1, {data[11:0], data[23:12]} Bit[1]: quarter_seq High half sequence Used to adjust the low 24-bits data sequence = 1'b0, data[47:24], = 1'b1, {data[35:24], data[47:36]} Bit[0]: rgb_seq Total sequence = 1'b0, data[47:0], = 1'b1, {data[11:0], data[23:12], data[35:24], data[47:36]}
0x3216	LP_DELAY	0x04	RW	LP00--LP11 Delay Cycle When hs_zero Sync Enable
0x3217	MIPI_DATA_TAG0	0x30	RW	Data_ID Tag Transmitted in Virtual Channel 0 for Supporting "Same Image Data Transmit in Different Virtual Channel With Different Data_ID Tag
0x3218	MIPI_DATA_TAG1	0x6C	RW	Data_ID Tag Transmitted in Virtual Channel 1 for Supporting "Same Image Data Transmit in Different Virtual Channel With Different Data_ID Tag

table A-2 sensor control registers (sheet 24 of 42)

address	register name	default value	R/W	description
0x3219	MIPI_DATA_TAG2	0xAC	RW	Data_ID Tag Transmitted in Virtual Channel 2 for Supporting "Same Image Data Transmit in Different Virtual Channel With Different Data_ID Tag
0x321A	MIPI_DATA_TAG3	0xEC	RW	Data_ID Tag Transmitted in Virtual Channel 3 for Supporting "Same Image Data Transmit In Different Virtual Channel With Different Data_ID Tag
0x321B	USE_VFIFO_TYPE	0x01	RW	Use the Size Signals (12, 10, and 8) from VFIFO
0x3230	LVDS_R0	0x2A	RW	Bit[7]: Not used Bit[6]: sync_cod_man Sync code manual enable Bit[5]: syncd_en Bit[4]: lvds_pclk_inv Invert LVDS pclk_o Bit[3]: r_chid_en Channel ID enable in sync per lane mode Bit[2]: lvds_f CCIR parameter F Bit[1]: sav_first_en 0: EAV first 1: SAV first Bit[0]: sync_code_mod (fixed to 1) Sync code per lane
0x3231	LVDS_R2	0x00	RW	Dummy Data0 High Nibble
0x3232	LVDS_R3	0x80	RW	Dummy Data0 Low Byte
0x3233	LVDS_R4	0x00	RW	Dummy Data1 High Nibble
0x3234	LVDS_R5	0x10	RW	Dummy Data1 Low Byte
0x3235	LVDS_R6	0xAA	RW	frame_st
0x3236	LVDS_R7	0x55	RW	frame_ed
0x3237	LVDS_R8	0x99	RW	line_st
0x3238	LVDS_R9	0x66	RW	line_ed
0x3239	LVDS_RA	0x08	RW	Bit[7:4]: Not used Bit[3]: bit_flip Bit[2]: Not used Bit[1]: ln2_sel Bit[0]: Not used

table A-2 sensor control registers (sheet 25 of 42)

address	register name	default value	R/W	description
0x323A	LVDS_RB	0x88	RW	Bit[7]: sleep_en Bit[6]: Not used Bit[5]: frame_rst_en Bit[4:0]: ln_end_dly
0x323B	LVDS_RC	0x00	RW	r_blk_time High Nibble
0x323C	LVDS_RD	0x00	RW	r_blk_time Low Byte
0x323D	LVDS_LANE_NR	0x03	RW	Number of Active LVDS Lanes
0x3250	ISP_DP_CONF1	0x33	RW	Bit[7]: dpc_bc_en Black pixel correction enable in DPC Bit[6]: dpc_wc_en White pixel correction enable in DPC Bit[5]: isp_out_window_en (active high, default high) ISP output window crop enable Bit[4]: comb_en DCG combine enable Bit[3]: lenc_en Enable lens correction Bit[2]: otp_en Defect pixel tagging enable Bit[1]: awb_gain_en AWB_gain enable Bit[0]: isp_en (active high, default high) ISP enable
0x3251	ISP_DP_SPARE	0x00	RW	isp_dp_spare
0x3252	ISP_SETTING	0x20	RW	Bit[7:6]: Not used Bit[5]: vsync_in_sel 0: sensor_core 1: black_row_end Bit[4]: vsync_out_sel 0: sensor_core 1: pre_isp Bit[3:2]: Not used Bit[1:0]: cfa_pattern 0: Mirror 1: Flip

table A-2 sensor control registers (sheet 26 of 42)

address	register name	default value	R/W	description
0x3253	PRE_CTRL0	0x00	RW	Bit[7]: test_mode_en Pre_ISP test mode enable Bit[6]: rolling_lines Pre_ISP rolling lines enable Bit[5]: transport_mode Pre_ISP transport mode enable Bit[4]: sq_bw Pre_ISP square black/white enable Bit[3:2]: color_bar Pre_ISP color bar style Bit[1:0]: img_sel Pre_ISP test image select 00: Bar 01: Rand 10: Square 11: Chart
0x3255	PRE_CTRL2	0x01	RW	Bit[7]: pre_force_cg_bit_man Pre_ISP force CG bit manual override enable Bit[6]: pre_force_cg_bit Pre_ISP force CG bit value if manual override is enabled Bit[5]: Test Pre_ISP test Low byte to 0 Bit[4]: rand_img Pre_ISP rand image same seed enable Bit[3:0]: rand_img_seed Pre_ISP rand image seed
0x3270	DCG_CTRL	0x01	RW	Bit[7:1]: Not used Bit[0]: dcg_dither_en Enable dithering of input pixel to DCG
0x3271	DCG_THRE_LOW	0x60	RW	DCG Combine Threshold Low
0x3272	DCG_THRE_HIGH	0xC0	RW	DCG Combine Threshold High
0x3273	BLC_TARGET_HDR_H	0x00	RW	HDR Dark Level Target, High Nibble
0x3274	BLC_TARGET_HDR_L	0x80	RW	HDR Dark Level Target, Low Byte
0x3275	MIN_PIXEL_NUMBER	0x20	RW	Minimum Number of Pixels Per Bin × 32
0x3276	STABLE_RANGE1	0x02	RW	Stable Range 1
0x3277	STABLE_RANGE2	0x08	RW	Stable Range 2
0x3278	UPDATE_STEP	0x10	RW	Filter Step

table A-2 sensor control registers (sheet 27 of 42)

address	register name	default value	R/W	description
0x3279	OFFSET_RANGE_H	0x04	RW	Offset Range, High Byte
0x327A	OFFSET_RANGE_L	0x00	RW	Offset Range, Low Byte
0x327B	STAT_RANGE	0x03	RW	Statistic Range
0x327C	RATIO_RANGE	0x10	RW	Ratio Range
0x327D	STAT_THRE_LOW	0x60	RW	Statistic Low Threshold
0x327E	STAT_THRE_HIGH	0xC0	RW	Statistic High Threshold
0x327F	MIN_BIN_DIST	0x03	RW	Minimum Bin Distance for Statistics
0x3330	LENC_RED_X0_H	0x03	RW	Red Center Horizontal Position (X0) High Byte
0x3331	LENC_RED_X0_L	0xC8	RW	Red Center Horizontal Position (X0) Low Byte
0x3332	LENC_RED_Y0_H	0x02	RW	Red Center Vertical Position (Y0) High Byte
0x3333	LENC_RED_Y0_L	0x24	RW	Red Center Vertical Position (Y0) Low Byte
0x3334	LENC_RED_A1	0x00	RW	Red Parameter A1
0x3335	LENC_RED_A2	0x00	RW	Red Parameter A2
0x3336	LENC_RED_B1	0x00	RW	Red Parameter B1
0x3337	LENC_RED_B2	0x00	RW	Red Parameter B2
0x3338	LENC_GRN_X0_H	0x03	RW	Green Center Horizontal Position (X0) High Byte
0x3339	LENC_GRN_X0_L	0xC8	RW	Green Center Horizontal Position (X0) Low Byte
0x333A	LENC_GRN_Y0_H	0x02	RW	Green Center Vertical Position (Y0) High Byte
0x333B	LENC_GRN_Y0_L	0x24	RW	Green Center Vertical Position (Y0) Low Byte
0x333C	LENC_GRN_A1	0x00	RW	Green Parameter A1
0x333D	LENC_GRN_A2	0x00	RW	Green Parameter A2
0x333E	LENC_GRN_B1	0x00	RW	Green Parameter B1
0x333F	LENC_GRN_B2	0x00	RW	Green Parameter B2
0x3340	LENC_BLU_X0_H	0x03	RW	Blue Center Horizontal Position (X0) High Byte
0x3341	LENC_BLU_X0_L	0xC8	RW	Blue Center Horizontal Position (X0) Low Byte
0x3342	LENC_BLU_Y0_H	0x02	RW	Blue Center Vertical Position (Y0) High Byte
0x3343	LENC_BLU_Y0_L	0x24	RW	Blue Center Vertical Position (Y0) Low Byte
0x3344	LENC_BLU_A1	0x00	RW	Blue Parameter A1

table A-2 sensor control registers (sheet 28 of 42)

address	register name	default value	R/W	description
0x3345	LENC_BLU_A2	0x00	RW	Blue Parameter A2
0x3346	LENC_BLU_B1	0x00	RW	Blue Parameter B1
0x3347	LENC_BLU_B2	0x00	RW	Blue Parameter B2
0x3348	LENC_CTRL	0x40	RW	Bit[7]: Not used Bit[6]: lenc_bias_plus Add bias back after LENC Bit[5:4]: real_gain_sel Select real gain to use for coefficient adjustment 00: HGC 01: LCG 1x: Not used Bit[3]: coef_man_en Override LENC gain coefficient with lenc_coef_man Bit[2]: gcoef_en Enables gain coefficient adjustment Bit[1]: quad_acc_en Bit[0]: rnd_en Adds random bits
0x3349	LENC_COEF_THRE	0x00	RW	Coefficient Threshold (Minimum Level of Coefficient Gain) Format: 1.7, Max: 1.0
0x334A	LENC_GAIN_THRE1_H	0x00	RW	ISP Real Gain Threshold Low (No Sub-LSB) High Byte
0x334B	LENC_GAIN_THRE1_L	0x00	RW	ISP Real Gain Threshold Low (No Sub-LSB) Low Byte
0x334C	LENC_GAIN_THRE2_H	0x00	RW	ISP Real Gain Threshold High (No Sub-LSB) High Byte
0x334D	LENC_GAIN_THRE2_L	0x00	RW	ISP Real Gain Threshold High (No Sub-LSB) Low Byte
0x334E	LENC_COEF_MAN	0x80	RW	Manual Coefficient Scaling Parameter, Format: 1.7, Max: 1.0
0x3360	R_GAIN_HCG_H	0x01	RW	Gain High Bits for HCG Channel Red Component
0x3361	R_GAIN_HCG_L	0x00	RW	Gain Low Bits for HCG Channel Red Component
0x3362	GR_GAIN_HCG_H	0x01	RW	Gain High Bits for HCG Channel Greenr Component
0x3363	GR_GAIN_HCG_L	0x00	RW	Gain Low Bits for HCG Channel Greenr Component

table A-2 sensor control registers (sheet 29 of 42)

address	register name	default value	R/W	description
0x3364	GB_GAIN_HCG_H	0x01	RW	Gain High Bits for HCG Channel Greenb Component
0x3365	GB_GAIN_HCG_L	0x00	RW	Gain Low Bits for HCG Channel Greenb Component
0x3366	B_GAIN_HCG_H	0x01	RW	Gain High Bits for HCG Channel Blue Component
0x3367	B_GAIN_HCG_L	0x00	RW	Gain Low Bits for HCG Channel Blue Component
0x3368	R_GAIN_LCG_H	0x01	RW	Gain High Bits for LCG Channel Red Component
0x3369	R_GAIN_LCG_L	0x00	RW	Gain Low Bits for LCG Channel Red Component
0x336A	GR_GAIN_LCG_H	0x01	RW	Gain High Bits for LCG Channel Greenr Component
0x336B	GR_GAIN_LCG_L	0x00	RW	Gain Low Bits for LCG Channel Greenr Component
0x336C	GB_GAIN_LCG_H	0x01	RW	Gain High Bits for LCG Channel Greenb Component
0x336D	GB_GAIN_LCG_L	0x00	RW	Gain Low Bits for LCG Channel Greenb Component
0x336E	B_GAIN_LCG_H	0x01	RW	Gain High Bits for LCG Channel Blue Component
0x336F	B_GAIN_LCG_L	0x00	RW	Gain Low Bits for LCG Channel Blue Component
0x3378	R_OFFSET_HCG_H	0x00	RW	Offset High Bits for HCG Channel Red Component
0x3379	R_OFFSET_HCG_M	0x00	RW	Offset Medium Bits for HCG Channel Red Component
0x337A	R_OFFSET_HCG_L	0x00	RW	Offset Low Bits for HCG Channel Red Component
0x337B	GR_OFFSET_HCG_H	0x00	RW	Offset High Bits for HCG Channel Greenr Component
0x337C	GR_OFFSET_HCG_M	0x00	RW	Offset Medium Bits for HCG Channel Greenr Component
0x337D	GR_OFFSET_HCG_L	0x00	RW	Offset Low Bits for HCG Channel Greenr Component
0x337E	GB_OFFSET_HCG_H	0x00	RW	Offset High Bits for HCG Channel Greenb Component

table A-2 sensor control registers (sheet 30 of 42)

address	register name	default value	R/W	description
0x337F	GB_OFFSET_HCG_M	0x00	RW	Offset Medium Bits for HCG Channel Greenb Component
0x3380	GB_OFFSET_HCG_L	0x00	RW	Offset Low Bits for HCG Channel Greenb Component
0x3381	B_OFFSET_HCG_H	0x00	RW	Offset High Bits for HCG Channel Blue Component
0x3382	B_OFFSET_HCG_M	0x00	RW	Offset Medium Bits for HCG Channel Blue Component
0x3383	B_OFFSET_HCG_L	0x00	RW	Offset Low Bits for HCG Channel Blue Component
0x3384	R_OFFSET_LCG_H	0x00	RW	Offset High Bits for LCG Channel Red Component
0x3385	R_OFFSET_LCG_M	0x00	RW	Offset Medium Bits for LCG Channel Red Component
0x3386	R_OFFSET_LCG_L	0x00	RW	Offset Low Bits for LCG Channel Red Component
0x3387	GR_OFFSET_LCG_H	0x00	RW	Offset High Bits for LCG Channel Greenr Component
0x3388	GR_OFFSET_LCG_M	0x00	RW	Offset Medium Bits for LCG Channel Greenr Component
0x3389	GR_OFFSET_LCG_L	0x00	RW	Offset Low Bits for LCG Channel Greenr Component
0x338A	GB_OFFSET_LCG_H	0x00	RW	Offset High Bits for LCG Channel Greenb Component
0x338B	GB_OFFSET_LCG_M	0x00	RW	Offset Medium Bits for LCG Channel Greenb Component
0x338C	GB_OFFSET_LCG_L	0x00	RW	Offset Low Bits for LCG Channel Greenb Component
0x338D	B_OFFSET_LCG_H	0x00	RW	Offset High Bits for LCG Channel Blue Component
0x338E	B_OFFSET_LCG_M	0x00	RW	Offset Medium Bits for LCG Channel Blue Component
0x338F	B_OFFSET_LCG_L	0x00	RW	Offset Low Bits for LCG Channel Blue Component

table A-2 sensor control registers (sheet 31 of 42)

address	register name	default value	R/W	description
0x33F5	CTRL_DPC_00_HCG	0x14	RW	Bit[7:6]: Not used Bit[5]: Tail enable Crosscluster must also be enabled Bit[4]: Saturate crosscluster enable Crosscluster must also be enabled Bit[3]: 3x3 cluster enable Bit[2]: Crosscluster enable Bit[1]: General tail enable Three horizontal connected clusters with one of the pixels exceeding the saturation value Bit[0]: Manual mode enable
0x33F6	CTRL_DPC_01_HCG	0x0F	RW	Bit[7:4]: Saturate pixel saturation threshold Bit[3]: Different channel white pixel correction enable Bit[2]: Different channel black pixel correction enable Bit[1]: Same channel white pixel correction enable Bit[0]: Same channel black pixel correction enable
0x33F7	CTRL_DPC_02_HCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list0 Threshold value for white pixel detection in manual mode
0x33F8	CTRL_DPC_03_HCG	0x02	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list1 Threshold value for white pixel detection in manual mode
0x33F9	CTRL_DPC_04_HCG	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list2 Threshold value for white pixel detection in manual mode
0x33FA	CTRL_DPC_05_HCG	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list3 Threshold value for white pixel detection in manual mode
0x33FB	CTRL_DPC_06_HCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern thresholds
0x33FC	CTRL_DPC_07_HCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern step
0x33FD	CTRL_DPC_08_HCG	0x0C	RW	Bit[7:4]: Not used Bit[3:0]: More connection case thresholds

table A-2 sensor control registers (sheet 32 of 42)

address	register name	default value	R/W	description
0x33FE	CTRL_DPC_09_HCG	0x00	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list0 DPC level is used to remove different types of clusters. Higher levels mean more defective clusters removed, but image quality will worsen
0x33FF	CTRL_DPC_10_HCG	0x01	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list1
0x3400	CTRL_DPC_11_HCG	0x02	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list2
0x3401	CTRL_DPC_12_HCG	0x03	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list3
0x3402	CTRL_DPC_13_HCG	0x03	RW	Bit[7]: Not used Bit[6:0]: Gain list0
0x3403	CTRL_DPC_14_HCG	0x0F	RW	Bit[7]: Not used Bit[6:0]: Gain list1
0x3404	CTRL_DPC_15_HCG	0x3F	RW	Bit[7]: Not used Bit[6:0]: Gain list2
0x3405	CTRL_DPC_16_HCG	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Matching thresholds If a similar pattern in the neighbor of the central defect pixel is found, this value will be used to replace the current defect pixel. This threshold is used to determine similarity between pixels. If the difference between two pixels is larger than this threshold, the two are not considered similar. Larger threshold will maintain more image detail.
0x3406	CTRL_DPC_17_HCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Status thresholds A pixel is marked as defective if the original and recovered value is larger than this threshold. More defective pixels will be removed with a larger threshold while removing image details.
0x3407	CTRL_DPC_18_HCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: wb_th_ ratio Ratio of white threshold and black threshold

table A-2 sensor control registers (sheet 33 of 42)

address	register name	default value	R/W	description
0x3408	CTRL_DPC_19_HCG	0x00	RW	Bit[7:1]: Not used Bit[0]: Clip interpolate G enable Controls whether or not to remove defective pixels in the B or R channel when G channel is saturated 0: Disable 1: Enable
0x3409	CTRL_DPC_20_HCG	0x03	RW	Bit[7:2]: Not used Bit[1:0]: edge_opt Image boundary process option 00: Pad zero to remove white pixels 01: Pad max value to remove black pixels 10: Duplicate the adjacent same channel data for padding 11: Duplicate the upper same channel data for padding
0x340A	CTRL_DPC_00_LCG	0x14	RW	Bit[7:6]: Not used Bit[5]: Tail enable Crosscluster must also be enabled Bit[4]: Saturate crosscluster enable Crosscluster must also be enabled Bit[3]: 3x3 cluster enable Bit[2]: Crosscluster enable Bit[1]: General tail enable Three horizontal connected clusters with one of the pixels exceeding the saturation value Bit[0]: Manual mode enable
0x340B	CTRL_DPC_01_LCG	0x0F	RW	Bit[7:4]: Saturate pixel saturation threshold Bit[3]: Different channel white pixel correction enable Bit[2]: Different channel black pixel correction enable Bit[1]: Same channel white pixel correction enable Bit[0]: Same channel black pixel correction enable
0x340C	CTRL_DPC_02_LCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list0 Threshold value for white pixel detection in manual mode

table A-2 sensor control registers (sheet 34 of 42)

address	register name	default value	R/W	description
0x340D	CTRL_DPC_03_LCG	0x02	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list1 Threshold value for white pixel detection in manual mode
0x340E	CTRL_DPC_04_LCG	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list2 Threshold value for white pixel detection in manual mode
0x340F	CTRL_DPC_05_LCG	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list3 Threshold value for white pixel detection in manual mode
0x3410	CTRL_DPC_06_LCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern thresholds
0x3411	CTRL_DPC_07_LCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern step
0x3412	CTRL_DPC_08_LCG	0x0C	RW	Bit[7:4]: Not used Bit[3:0]: More connection case thresholds
0x3413	CTRL_DPC_09_LCG	0x00	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list0 DPC level is used to remove different types of clusters. Higher levels mean more defective clusters removed, but image quality will worsen
0x3414	CTRL_DPC_10_LCG	0x01	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list1
0x3415	CTRL_DPC_11_LCG	0x02	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list2
0x3416	CTRL_DPC_12_LCG	0x03	RW	Bit[7:2]: Not used Bit[1:0]: DPC level list3
0x3417	CTRL_DPC_13_LCG	0x03	RW	Bit[7]: Not used Bit[6:0]: Gain list0
0x3418	CTRL_DPC_14_LCG	0x0F	RW	Bit[7]: Not used Bit[6:0]: Gain list1
0x3419	CTRL_DPC_15_LCG	0x3F	RW	Bit[7]: Not used Bit[6:0]: Gain list2

table A-2 sensor control registers (sheet 35 of 42)

address	register name	default value	R/W	description
0x341A	CTRL_DPC_16_LCG	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Matching thresholds If a similar pattern in the neighbor of the central defect pixel is found, this value will be used to replace the current defect pixel. This threshold is used to determine similarity between pixels. If the difference between two pixels is larger than this threshold, the two are not considered similar. Larger threshold will maintain more image detail.
0x341B	CTRL_DPC_17_LCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Status thresholds A pixel is marked as defective if the original and recovered value is larger than this threshold. More defective pixels will be removed with a larger threshold while removing image details.
0x341C	CTRL_DPC_18_LCG	0x04	RW	Bit[7:4]: Not used Bit[3:0]: wb_th_ ratio Ratio of white threshold and black threshold
0x341D	CTRL_DPC_19_LCG	0x00	RW	Bit[7:1]: Not used Bit[0]: Clip interpolate G enable Controls whether or not to remove defective pixels in the B or R channel when G channel is saturated 0: Disable 1: Enable
0x341E	CTRL_DPC_20_LCG	0x03	RW	Bit[7:2]: Not used Bit[1:0]: edge_opt Image boundary process option 00: Pad zero to remove white pixels 01: Pad max value to remove black pixels 10: Duplicate the adjacent same channel data for padding 11: Duplicate the upper same channel data for padding
0x3426	CTRL_DPC_21_HCG	–	R	Bit[7]: Not used Bit[6:0]: Black thresholds

table A-2 sensor control registers (sheet 36 of 42)

address	register name	default value	R/W	description
0x3427	CTRL_DPC_22_HCG	–	R	Bit[7:5]: Not used Bit[4:0]: White thresholds
0x3428	CTRL_DPC_23_HCG	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 1
0x3429	CTRL_DPC_24_HCG	–	R	Bit[7:6]: Not used Bit[5:0]: Threshold 2
0x342A	CTRL_DPC_25_HCG	–	R	Bit[7]: Not used Bit[6:0]: Threshold 3
0x342B	CTRL_DPC_26_HCG	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 4
0x342C	CTRL_DPC_27_HCG	–	R	Bit[7:4]: Not used Bit[3:0]: Level
0x342D	CTRL_DPC_21_LCG	–	R	Bit[7]: Not used Bit[6:0]: Black thresholds
0x342E	CTRL_DPC_22_LCG	–	R	Bit[7:5]: Not used Bit[4:0]: White thresholds
0x342F	CTRL_DPC_23_LCG	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 1
0x3430	CTRL_DPC_24_LCG	–	R	Bit[7:6]: Not used Bit[5:0]: Threshold 2
0x3431	CTRL_DPC_25_LCG	–	R	Bit[7]: Not used Bit[6:0]: Threshold 3
0x3432	CTRL_DPC_26_LCG	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 4
0x3433	CTRL_DPC_27_LCG	–	R	Bit[7:4]: Not used Bit[3:0]: Level
0x3440	R_CTRL00	0x00	RW	Manual X Start Coordinate High Byte
0x3441	R_CTRL01	0x00	RW	Manual X Start Coordinate Low Byte
0x3442	R_CTRL02	0x00	RW	Manual Y Start Coordinate High Byte
0x3443	R_CTRL03	0x00	RW	Manual Y Start Coordinate Low Byte
0x3444	R_CTRL04	0x02	RW	Manual Window Width High Byte
0x3445	R_CTRL05	0xF0	RW	Manual Window Width Low Byte
0x3446	R_CTRL06	0x02	RW	Manual Window Height High Byte
0x3447	R_CTRL07	0x08	RW	Manual Window Height Low Byte
0x3448	R_CTRL08	0x00	RW	Control Bit

table A-2 sensor control registers (sheet 37 of 42)

address	register name	default value	R/W	description
0x3449	R_CTRL09	–	R	Read Out Pixel Count High Byte
0x344A	R_CTRL0A	–	R	Read Out Pixel Count Low Byte
0x344B	R_CTRL0B	–	R	Read Out Line Count High Byte
0x344C	R_CTRL0C	–	R	Read Out Line Count Low Byte
0x3460	GROUP_LENGTH0	0x40	RW	Number of Registers for Group 0, Total Sum of 4 Groups Is Limited to 256
0x3461	GROUP_LENGTH1	0x40	RW	Number of Registers for Group 1
0x3462	GROUP_LENGTH2	0x40	RW	Number of Registers for Group 2
0x3463	GROUP_LENGTH3	0x40	RW	Number of Registers for Group 3
0x3464	GROUP_CTRL	0x03	RW	Bit[7]: Not used Bit[6]: launch_now Launch immediately when single_start i set Bit[5]: launch_pre_sof Launch before sensor core SOF, if single_start is set Bit[4]: launch_post_sof Launch after sensor core SOF, if single_start is set Bit[3:2]: first_grp_sel Main group select for hold and launch operation. Also used as the first group in auto mode. Bit[1:0]: second_grp_sel Used as second group in auto mode
0x3465	FIRST_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by First Group Select
0x3466	SECOND_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by Second Group Select
0x3467	OPERATION_CTRL	0x02	RW	Bit[7:2]: Not used Bit[1]: auto_mode Switches automatically between first and second groups using frame counts Bit[0]: single_start Launch only once. Reset by logic after done. Overridden by auto_mode.
0x3468	EMB_START_ADDR0_H	0x30	RW	High Address for the First Embedded Data Range 0

table A-2 sensor control registers (sheet 38 of 42)

address	register name	default value	R/W	description
0x3469	EMB_START_ADDR0_L	0x00	RW	Low Address for the First Embedded Data Range 0
0x346A	EMB_END_ADDR0_H	0x35	RW	High Address for the Last Embedded Data Range 0
0x346B	EMB_END_ADDR0_L	0x00	RW	Low Address for the Last Embedded Data Range 0
0x346C	ACTIVE_GROUP_NR	–	R	Indicates Which Group is Active
0x346D	FRAME_CNT_ACTIVE	–	R	The Number of Frames With the Current Group, Valid Only in Auto Mode
0x3480	MIPI_CTRL0	0x00	RW	Bit[7:5]: pgm_vcm Bit[4:3]: pgm_lptx Bit[2:1]: pgm_lphi Adjust LPTX output voltage Bit[0]: bp_c_hs_en_lat Bypass ck_hs_en without mipi_pclk's latching
0x3481	MIPI_CTRL1	0x00	RW	Bit[7:5]: skew_clk Bit[4]: dis_clk_lane Bit[3:0]: dis_d_lane
0x3482	MIPI_D_SKEW01	0x00	RW	Bit[7]: Not used Bit[6:4]: skew_d1 Bit[3]: Not used Bit[2:0]: skew_d0
0x3483	MIPI_D_SKEW23	0x00	RW	Bit[7]: Not used Bit[6:4]: skew_d3 Bit[3]: Not used Bit[2:0]: skew_d2
0x3485	MIPI_CTRL3	0x00	RW	Bit[7]: mipi_man Manual MIPI lane control settings (mipi_ctrl1 bit[4:0]) Bit[6]: mipi_data_valid_sel 0: Lane0 data valid used for all lanes 1: Lane-specific LVDS data valid Bit[5:4]: Ictl IVREF input bias current control Bit[3:0]: bgr_vref
0x3486	MIPI_CONF	0x00	RW	Bit[7:5]: Not used Bit[4:2]: emb_line_nu Bit[1]: fun_4x_y_en Bit[0]: ul_tx_fun_en

table A-2 sensor control registers (sheet 39 of 42)

address	register name	default value	R/W	description
0x3487	MIPI_PADS_DIR	0x00	RW	0: Output 1: Input (for TM)
0x3488	DVP_PWR	0x00	RW	Bit[7:6]: Not used Bit[5]: pwdn_out Drive-value during power down for D-pads, HREF, VSYNC, and PCLK Bit[4]: pwdn_oe Drive-enable during power down for D-pads, HREF, VSYNC, and PCLK Bit[3:2]: pclk_pwr Drive-strength for PCLK when active Bit[1:0]: d_pwr Drive-strength for data-pins, HREF, and VSYNC pins when active
0x3489	GPIO_OE	0x00	RW	GPIO Output Enable Bit[7:2]: Not used Bit[1]: GPIO1 output enable Bit[0]: GPIO0 output enable
0x348A	GPIO_O	0x00	RW	GPIO Output Value Bit[1]: GPIO1 output value Bit[0]: GPIO0 output value
0x348B	GPIO_CTRL	0x04	RW	Bit[7:5]: gpio_sel0 000: Not used 001: Row trigger 010: Not used 011: Not used 100: PLL1 lock 101: PLL2 lock 110: Watchdog pulse Bit[4:3]: gpio_sel1 00: Not used 01: VSYNC 10: Not used 11: Sequencer GPIO1 Bit[2]: Ien GPIO input enable (must be 1 for gpio_in to be valid) Bit[1:0]: Pwr Driving strength for GPIO pads
0x348C	TRIGGER_ADDR_SL_H	0x00	RW	GPIO Row Trigger Address for samp_l High Byte
0x348D	TRIGGER_ADDR_SL_L	0x01	RW	GPIO Row Trigger Address for samp_l Low Byte
0x348E	GPIO_IN	–	R	GPIO Input Value

table A-2 sensor control registers (sheet 40 of 42)

address	register name	default value	R/W	description
0x348F	WDP_WIDTH	0x01	RW	Watchdog Pulse Width, Number of SCLK Cycles
0x34A0	OTP_PGM_CTRL	0x00	RW	Bit[7:1]: Not used Bit[0]: otp_pgm Write 1 to program OTP, auto reset
0x34A1	OTP_LOAD_CTRL	0x00	RW	Bit[7:1]: Not used Bit[0]: otp_rd Write 1 to read OTP, auto reset
0x34A2	OTP_PGM_PULSE	0x80	RW	control_program_strobe_pulse by 8×Tsclk
0x34A3	OTP_LOAD_PULSE	0x08	RW	control_load_strobe_pulse by Tsclk
0x34A4	OTP_MODE_CTRL	0x00	RW	Bit[7]: program_dis 1: Disable programing Bit[6]: mode_sel 0: Auto mode 1: Manual mode Bit[5:1]: Not used Bit[0]: bank_sram_switch Switch between using bank and SRAM 0: SRAM 1: Bank
0x34A5	OTP_CTRL	0x06	RW	Bit[7:6]: Not used Bit[5]: OTP_bist_select 0: Compare with SRAM 1: Compare with 0 Bit[4]: OTP_bist_en OTP BIST enable Bit[3]: Not used Bit[2]: OTP_pwup_load_data_en Read OTP data on power up Bit[1]: OTP_pwup_load_setting_en Load OTP at power up Bit[0]: OTP_sw_load_setting_en Enable soft-trigger for OTP load
0x34A7	OTP_PS2CS	0x03	RW	PS to CSB Time Control, by SCLK
0x34A8	OTP_ST_PT_H	0x00	RW	Start Address for Manual Mode High Byte
0x34A9	OTP_ST_PT_L	0x00	RW	Start Address for Manual Mode Low Byte
0x34AA	OTP_END_PT_H	0x01	RW	End Address for Manual Mode High Byte
0x34AB	OTP_END_PT_L	0xFF	RW	End Address for Manual Mode Low Byte
0x34AC	OTP_SETTING_ADR_ST_PT_H	0x00	RW	Start Address for Load Setting High Byte

table A-2 sensor control registers (sheet 41 of 42)

address	register name	default value	R/W	description
0x34AD	OTP_SETTING_ADR_ST_PT_L	0x10	RW	Start Address for Load Setting Low Byte
0x34AE	OTP_BASE_ADR_H	0x00	RW	OTP Base Address High Byte
0x34AF	OTP_BASE_ADR_L	0x00	RW	OTP Base Address Low Byte
0x34B0	OTP_BIST_ERR_ADR_H	–	R	OTP BIST Error Address High Byte
0x34B1	OTP_BIST_ERR_ADR_L	–	R	OTP BIST Error Address Low Byte
0x34B2	OTP_STATUS	–	R	Bit[7]: otp_pgm_o 0: Not used 1: Programming ongoing Bit[6]: otp_load_o 0: Not used 1: Load ongoing Bit[5]: otp_bist_err OTP BIST error Bit[4]: otp_bist_done OTP BIST done Bit[3:0]: Not used
0x34B3	OTP_CRC0	0x00	RW	OTP Content CRC Byte 0
0x34B4	OTP_CRC1	0x00	RW	OTP Content CRC Byte 1
0x34B5	OTP_CRC2	0x00	RW	OTP Content CRC Byte 2
0x34B6	OTP_CRC3	0x00	RW	OTP Content CRC Byte 3
0x7FF0	SCCB_R0	0x00	RW	Bit[7:4]: Not used Bit[3]: sda_dly_en Bit[2:0]: sda_dly
0x7FF1	SCCB_R1	0x12	RW	Bit[7:5]: Not used Bit[4]: en_sccb_addr_o_inc Bit[3]: sda_byp_sync 0: Not used 1: No sync for sda_i Bit[2]: r_scl_byp_sync 0: Not used 1: No sync for scl_i Bit[1]: r_msk_glitch Bit[0]: r_msk_stop
0x7FF2	SCCB_R2	0x00	RW	Bit[7:4]: r_sda_num Bit[3:0]: r_scl_num

table A-2 sensor control registers (sheet 42 of 42)

address	register name	default value	R/W	description
0x7FF3	SCCB_R3	0x00	RW	Bit[7]: Not used Bit[6]: ctrl_rst_mipisc Bit[5]: ctrl_rst_srb Bit[4]: ctrl_rst_sccb_s Bit[3]: ctrl_rst_pon_sccb_s Bit[2]: ctrl_rst_clkmod Bit[1]: ctrl_mipi_phy_rst_o Bit[0]: ctrl_pll_rst_o
0x7FF4	SCCB_R4	0x01	RW	Bit[7:5]: Not used Bit[4]: r_srb_clk_syn_en Bit[3]: pwup_dis2 Bit[2]: pwup_dis1 Bit[1]: pll_clk_sel Bit[0]: pwup_dis0
0x7FF5	SCCB_R5	0x01	RW	padclk_div
0x7FF6	SCCB_CRC_H	–	R	SCCB CRC High Byte
0x7FF7	SCCB_CRC_L	–	R	SCCB CRC Low Byte

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