OmniVision

datasheet

PRELIMINARY SPECIFICATION

1/3.06" color CMOS 13.2 megapixel (4224 x 3136) image sensor
with OmniBSI-3™ technology

OV13850

color CMOS 13.2 megapixel (4224 x 3136) image sensor with OmniBSI-3™ technology

datasheet (COB)
PRELIMINARY SPECIFICATION

version 1.2
october 2013

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- PC multimedia
- tablets

ordering information

- **OV13850-G04A** (color, chip probing, 200 µm backgrinding, reconstructed wafer with good die)

features

- 1.12 µm x 1.12 µm pixel with OmniBSI-3™ technology
- optical size of 1/3.06"
- 31.2° CRA for <6mm z-height
- programmable controls for frame rate, mirror and flip, cropping, and windowing
- support for image sizes: 13.2MP (4224x3136), 10MP (16:9 - 4224x2376), 4K2K (3840x2160), EIS 1080p (2112x1188), EIS 720p (1408x792), and more
- 13.2MP at 30 fps
- two-wire serial bus control (SCCB)
- strobe output to control flash
- 8kbits of embedded one-time programmable (OTP) memory (see **sidebar note**)
- two on-chip phase lock loops (PLLs)
- programmable controls: gain, exposure, frame rate, image size, horizontal mirror, vertical flip, cropping, and panning
- image quality controls: defect pixel correction, automatic black level calibration, lens shading correction, and alternate row HDR
- built-in temperature sensor
- suitable for module size of 8.5 mm x 8.5 mm x <6mm

note 3.3kbits are reserved for customer.

note pixel performance shown are target values. These values are subject to change based on real measurements.

key specifications (typical)

- **active array size:** 4224x3136
- **power supply:**
  - analog: 2.6 ~ 3.0V (2.8V nominal)
  - core: 1.14 ~ 1.26V (1.2V nominal)
  - I/O: 1.7 ~ 3.0V (1.8V or 2.8V nominal)
- **power requirements:**
  - active: 223mW
  - standby: 300µW
  - XSHUTDOWN: 1µW
- **temperature range:**
  - operating: -30°C to 85°C junction temperature
  - stable image: 0°C to 60°C junction temperature
- **output interfaces:** up to 4-lane MIPI serial output
- **output formats:** 10-bit RGB RAW
- **lens size:** 1/3.06"
- **input clock frequency:** 6 ~ 64 MHz
- **lens chief ray angle:** 31.2°
- **sensitivity:** TBD
- **max S/N ratio:** TBD
- **dynamic range:** TBD
- **pixel size:** 1.12 µm x 1.12 µm
- **dark current:** TBD
- **image area:** 4815 µm x 3678.3 µm
- **die dimensions:** 6210 µm x 5517 µm (COB), 6260 µm x 5567 µm (RW) (see **section 8** for details)

note COB refers to whole wafers with known good die and RW refers to singulated good die on a reconstructed wafer. Die size differs between COB and RW.

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pad numbers for the OV13850 image sensor. The die information is shown in section 8.

table 1-1 signal descriptions (sheet 1 of 3)

pad number	signal name	pad type	description
1	DVDD	reference	power for digital circuit
2	DOGND	ground	ground for I/O circuit
3	AGND	ground	ground for analog circuit
4	AGND	ground	ground for analog circuit
5	AVDD	power	power for analog circuit
6	AVDD	power	power for analog circuit
7	DVDD	reference	power for digital circuit
8	GPIO1	I/O	general purpose I/O
9	SID	input	SCCB ID select 0: SCCB device address 0x20 1: SCCB device address 0x6C
10	ILPWM	I/O	illumination control
11	GPIO	I/O	general purpose I/O
12	FSIN	I/O	frame sync input
13	FREX	I/O	frame exposure input
14	DOGND	ground	ground for I/O circuit
15	DOGND	ground	ground for I/O circuit
16	DVDD	reference	power for digital circuit
17	DVDD	reference	power for digital circuit
18	HREF	I/O	HREF output
19	SIOD	I/O	SCCB data
20	NC	–	no connect
21	SIOC	input	SCCB clock
22	NC	–	no connect
23	AVDD	power	power for analog circuit
24	DOVDD	power	power for I/O circuit

table 1-1 signal descriptions (sheet 2 of 3)

pad number	signal name	pad type	description
25	DOVDD	power	power for I/O circuit
26	DVDD	reference	power for digital circuit
27	DVDD	reference	power for digital circuit
28	DOGND	ground	ground for I/O circuit
29	DOGND	ground	ground for I/O circuit
30	ATEST0	reference	internal analog reference
31	DOGND	ground	ground for I/O circuit
32	DOGND	ground	ground for I/O circuit
33	DVDD	reference	power for digital circuit
34	DVDD	reference	power for digital circuit
35	AVDD	power	power for analog circuit
36	AVDD	power	power for analog circuit
37	AGND	ground	ground for analog circuit
38	AGND	ground	ground for analog circuit
39	AGND	ground	ground for analog circuit
40	AVDD	power	power for analog circuit
41	DOGND	ground	ground for I/O circuit
42	DVDD	reference	power for digital circuit
43	VH	reference	internal analog reference
44	VN	reference	internal analog reference
45	DOVDD	power	power for I/O circuit
46	XSHUTDOWN	input	reset and power down (active low with internal pull down resistor)
47	PWDNB	input	power down (active low with internal pull up resistor)
48	AGND	ground	ground for analog circuit
49	AVDD	power	power for analog circuit
50	TM	input	scan chain (active high with internal pull down resistor)
51	STROBE	I/O	strobe output
52	DOVDD	power	power for I/O circuit
53	MDP2	I/O	MIPI TX data lane 2 positive output

table 1-1 signal descriptions (sheet 3 of 3)

pad number	signal name	pad type	description
54	MDN2	I/O	MIPI TX data lane 2 negative output
55	EVDD	reference	power for MIPI TX circuit
56	MDP0	I/O	MIPI TX data lane 0 positive output
57	MDN0	I/O	MIPI TX data lane 0 negative output
58	EGND	ground	ground for MIPI TX circuit
59	PVDD	power	power for PLL circuit
60	EGND	ground	ground for MIPI TX circuit
61	EVDD	reference	power for MIPI TX circuit
62	MCP	I/O	MIPI TX clock lane positive output
63	MCN	I/O	MIPI TX clock lane negative output
64	EGND	ground	ground for MIPI TX circuit
65	MDP1	I/O	MIPI TX data lane 1 positive output
66	MDN1	I/O	MIPI TX data lane 1 negative output
67	EVDD	reference	power for MIPI TX circuit
68	MDP3	I/O	MIPI TX data lane 3 positive output
69	MDN3	I/O	MIPI TX data lane 3 negative output
70	DOGND	ground	ground for I/O circuit
71	VSYNC	I/O	VSYNC output
72	EXTCLK	input	system input clock
73	DOGND	ground	ground for I/O circuit
74	DOGND	ground	ground for I/O circuit
75	DVDD	reference	power for digital circuit
76	DVDD	reference	power for digital circuit

table 1-2 configuration under various conditions (sheet 1 of 2)

pad number	signal name	RESET[a]	after RESET release[b]	software standby	hardware standby[c]
8	GPIO1	high-z	input	high-z by default (configurable)	high-z by default (configurable)
9	SID	input	input	input	input
10	ILPWM	output zero	output zero by default (configurable)	output zero by default (configurable)	output zero by default (configurable)
11	GPIO	high-z	input	high-z by default (configurable)	high-z by default (configurable)
12	FSIN	high-z	input	high-z by default (configurable)	high-z by default (configurable)
13	FREX	high-z	input	high-z by default (configurable)	high-z by default (configurable)
18	HREF	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
19	SIOD	high-z	input	input	high-z
21	SIOC	high-z	input	input	high-z
30	ATEST0	high-z	open drain	open drain	high-z
43	VH	high-z	open drain	open drain	high-z
44	VN	high-z	open drain	open drain	high-z
46	XSHUTDOWN	input	input	input	input
47	PWDNB	input	input	input	input
50	TM	input	input	input	input
51	STROBE	output zero	output zero by default (configurable)	output zero by default (configurable)	output zero by default (configurable)
53	MDP2	high-z	high	high by default (configurable)	high by default (configurable)
54	MDN2	high-z	high	high by default (configurable)	high by default (configurable)
56	MDP0	high-z	high	high by default (configurable)	high by default (configurable)
57	MDN0	high-z	high	high by default (configurable)	high by default (configurable)
62	MCP	high-z	high	high by default (configurable)	high by default (configurable)

table 1-2 configuration under various conditions (sheet 2 of 2)

pad number	signal name	RESET[a]	after RESET release[b]	software standby	hardware standby[c]
63	MCN	high-z	high	high by default (configurable)	high by default (configurable)
65	MDP1	high-z	high	high by default (configurable)	high by default (configurable)
66	MDN1	high-z	high	high by default (configurable)	high by default (configurable)
68	MDP3	high-z	high	high by default (configurable)	high by default (configurable)
69	MDN3	high-z	high	high by default (configurable)	high by default (configurable)
71	VSYNC	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
72	EXTCLK	input	input	input	high-z

a. XSHUTDOWN = 0

b. XSHUTDOWN from 0 to 1

c. PWDNB = 0

figure 1-1 pad diagram

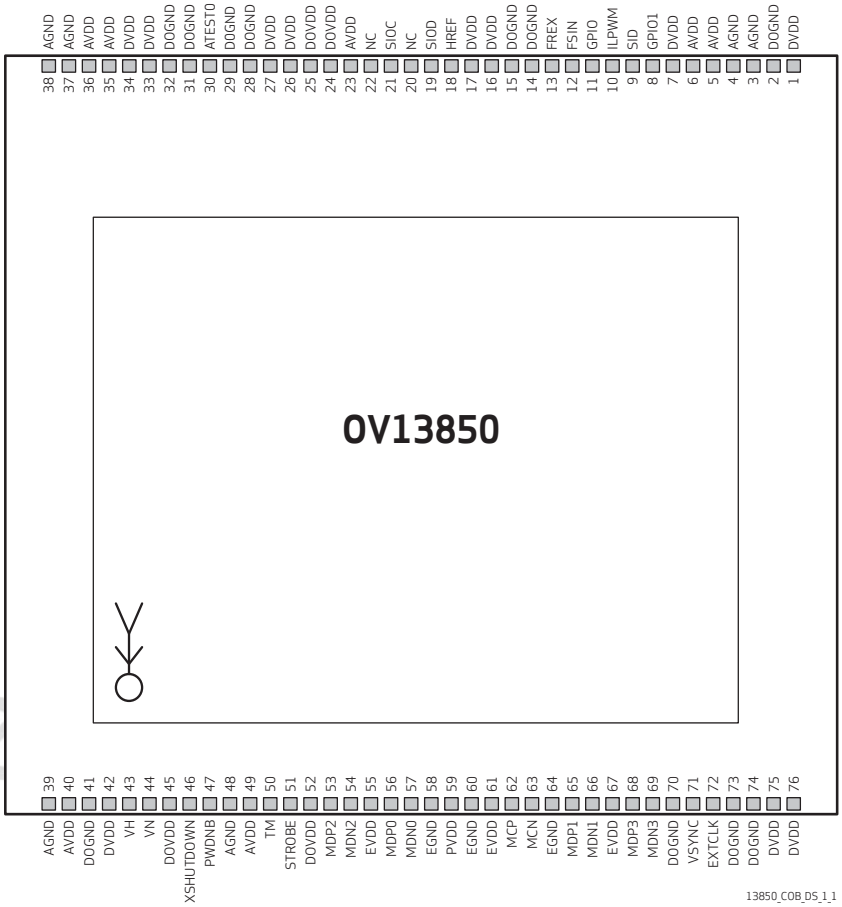


table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

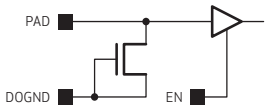
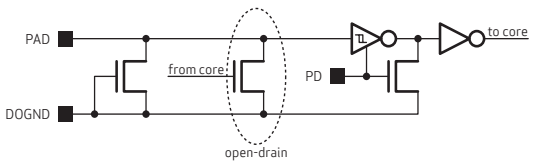
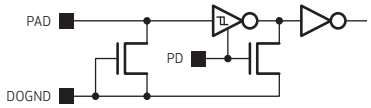
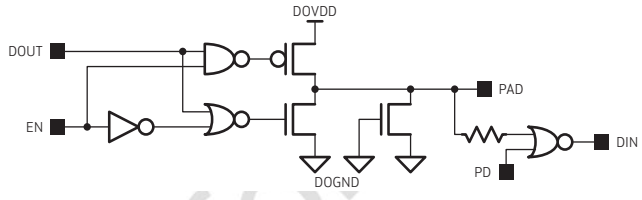
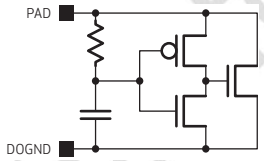
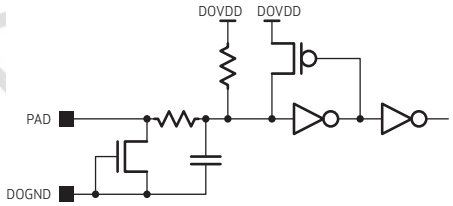
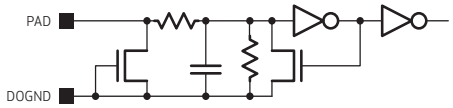
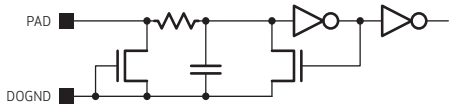
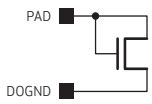
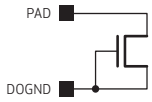
symbol	equivalent circuit
EXTCLK	
SIOD	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
SIOC	
VSYNC, HREF, STROBE, ILPWM, FREX, FSIN, GPIO, GPIO1	
AVDD, EVDD, DOVDD, DVDD, PVDD	
PWDNB	
TM, XSHUTDOWN	
SID	
VN, VH	
MCP, MCN, MDP0, MDN0, MDP1, MDN1, MDP2, MDN2, MDP3, MDN3, EGND, AGND, DOGND	

2 system level description

2.1 overview

The OV13850 (RAW RGB) image sensor is a low voltage, high performance 1/3.06-inch 13 megapixel CMOS image sensor that provides the functionality of a single 13 megapixel (4224X3136) camera using OmniBSI-3™ technology. It provides full-frame, sub-sampled, and windowed MIPI images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV13850 has an image array capable of operating at up to 30 frames per second (fps) in 10-bit 13 megapixel resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, white balance, defective pixel canceling, etc., are programmable through the SCCB interface.

In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

For customized information purposes, the OV13850 includes one-time programmable (OTP) memory. The OV13850 has four lanes of MIPI interface.

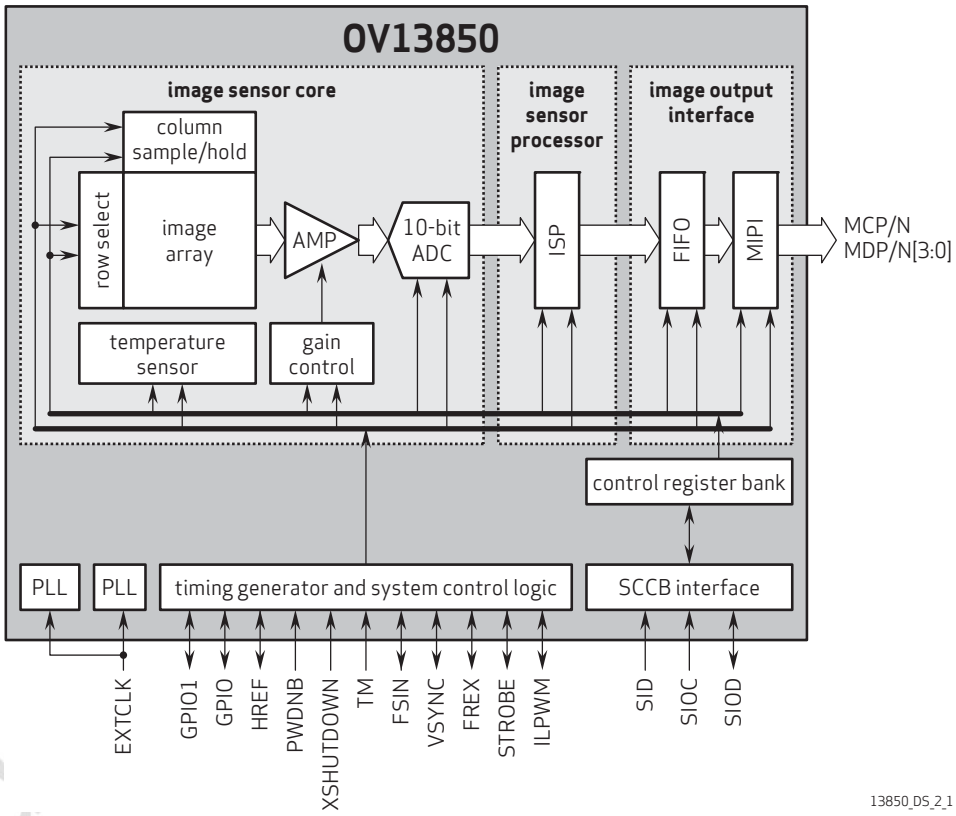
2.2 architecture

The OV13850 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV13850 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, precharging and sampling rows of the array sequentially. In the time between precharging and sampling a row, the charge in the pixels decrease with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV13850 block diagram



2.3 format and frame

The OV13850 supports RAW RGB output with 1/2/4 lane MIPI interfaces as listed in **table 2-1**.

table 2-1 format and frame rate

format	resolution	maximum output	methodology
13.2 megapixel	4224 x 3136	30 fps	full resolution
2x binning	2112x1568	60 fps	2x2 binning 1080p EIS 2112x1188 60fps by cropping 720p EIS 1408x792 60fps by cropping
10 megapixel (16:9)	4224x2376	30 fps	cropping

2.4 I/O control

I/O pads on the OV13850 can be configured as inputs or outputs. The output signals can come either from a data path or registers.

table 2-2 I/O control registers (sheet 1 of 2)

function	register	description
output drive capability control	0x3009	Bit[6:5]: I/O pad drive capability 00: 1x 01: 2x 10: 3x 11: 4x
VSYNC I/O control	0x3002	Bit[7]: input/output control for VSYNC pad 0: input 1: output
VSYNC output select	0x3008	Bit[7]: output selection for VSYNC pad 0: normal data path (vertical sync signal) 1: register control value
VSYNC output value	0x3005	Bit[7]: VSYNC output value
FREX I/O control	0x3002	Bit[4]: input/output control for FREX pad 0: input 1: output
FREX output select	0x3008	Bit[5]: output selection for FREX pad 0: normal data path 1: register control value
FREX output value	0x3005	Bit[4]: FREX output value
STROBE output select	0x3008	Bit[4]: output selection for STROBE pad 0: normal data path 1: register control value
STROBE output value	0x3005	Bit[2]: STROBE output value
HREF I/O control	0x3002	Bit[6]: input/output control for HREF pad 0: input 1: output
HREF output select	0x3008	Bit[6]: output selection for HREF pad 0: normal data path (horizontal sync signal) 1: register control value
HREF output value	0x3005	Bit[6]: HREF output value
FSIN I/O control	0x3002	Bit[3]: input/output control for FSIN pad 0: input 1: output

table 2-2 I/O control registers (sheet 2 of 2)

function	register	description
FSIN output select	0x3008	Bit[3]: output selection for FSIN pad 0: normal data path (illumination control signal) 1: register control value
FSIN output value	0x3005	Bit[3]: FSIN output value
GPIO I/O control	0x3002	Bit[0]: input/output control for GPIO pad 0: input 1: output
GPIO output select	0x3008	Bit[0]: output selection for GPIO pad 0: normal data path 1: register control value
GPIO output value	0x3005	Bit[0]: GPIO output value
GPIO1 I/O control	0x3002	Bit[1]: input/output control for GPIO1 pad 0: input 1: output
GPIO1 output select	0x3008	Bit[1]: output selection for GPIO1 pad 0: normal data path 1: register control value
GPIO1 output value	0x3005	Bit[1]: GPIO1 output value

2.5 MIPI interface

The OV13850 supports a 1, 2 and 4-lane MIPI extended D-PHY transmitter interface with a maximum data transfer rate of 1200 Mbps per lane with slew rate control.

figure 2-2 MIPI timing

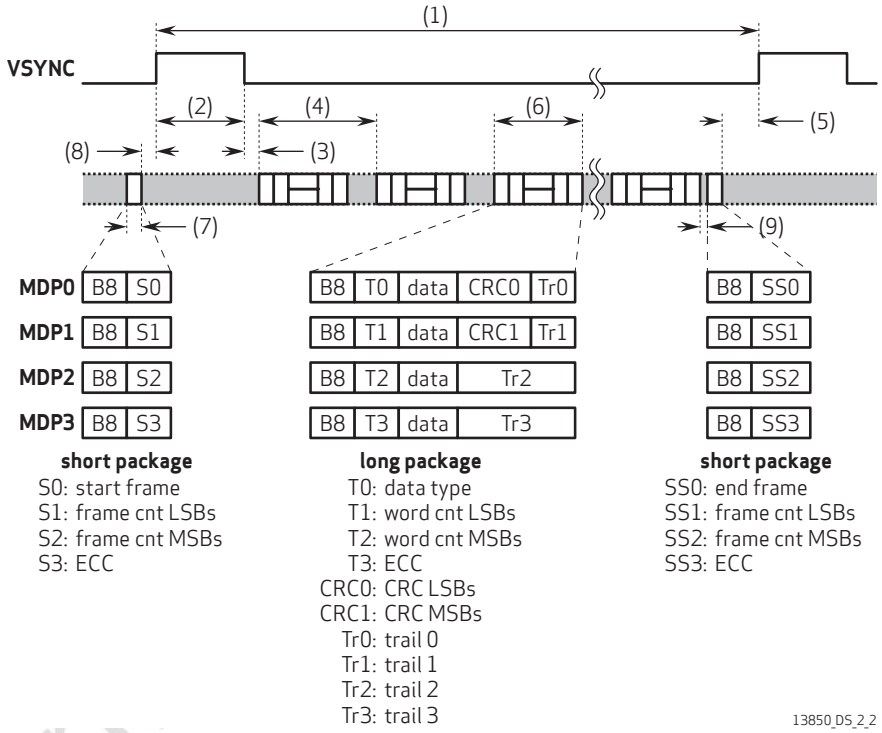


table 2-3 MIPI timing specifications

mode	timing
13 Megapixel 4208x3120 30 fps	(1) TBD tp (2) TBD tp (3) TBD tp (4) TBD tp (5) TBD tp (6) TBD tp (7) TBD tp (8) TBD tp (9) TBD tp where tp = Tsclk

2.6 power management

2.6.1 power up sequence

The OV13850 uses three power supplies: 2.8V AVDD, 1.8V DOVDD and 1.2V DVDD.

To avoid any glitch from a strong external noise source, OmniVision recommends controlling XSHUTDOWN or PWDNB by GPIO and tying the other pin to DOVDD.

Whether or not XSHUTDOWN is controlled by GPIO, the XSHUTDOWN rising cannot occur before AVDD or DOVDD.

table 2-4 power up sequence

case	XSHUTDOWN	PWDNB	power up sequence requirement
1	GPIO	DOVDD	Refer to **figure 2-3** 1. DOVDD rising must occur before DVDD rising 2. AVDD rising can occur before or after DOVDD rising 3. XSHUTDOWN rising must occur after AVDD, DOVDD and DVDD are stable
2	DOVDD	GPIO	Refer to **figure 2-4** 1. AVDD rising occurs before DOVDD rising 2. DOVDD rising occurs before DVDD 3. PWDNB rising occurs after DVDD rising

table 2-5 power up sequence timing constraints

constraint	label	min	max	unit
AVDD rising – DOVDD rising	t0	0	∞	ns
DOVDD rising – AVDD rising	t1			ns
AVDD or DOVDD rising, whichever is last – XSHUTDOWN rising	t2	0.0		ns
XSHUTDOWN rising – first CCI transaction	t3	8192		EXTCLK cycles
minimum number of EXTCLK cycles prior to the first CCI transaction	t4	8192		EXTCLK cycles
entering streaming mode – first frame start sequence (fixed part)	t5		10	ms
entering streaming mode – first frame start sequence (variable part)	t6	delay is the exposure time value		lines
AVDD or DOVDD, whichever is last – DVDD	t7	0.0	∞	ns
DVDD - PWDNB rising	t8	0	∞	ns
DVDD - XSHUTDOWN rising	t9	0	∞	ns

figure 2-3 power up sequence (case 1)

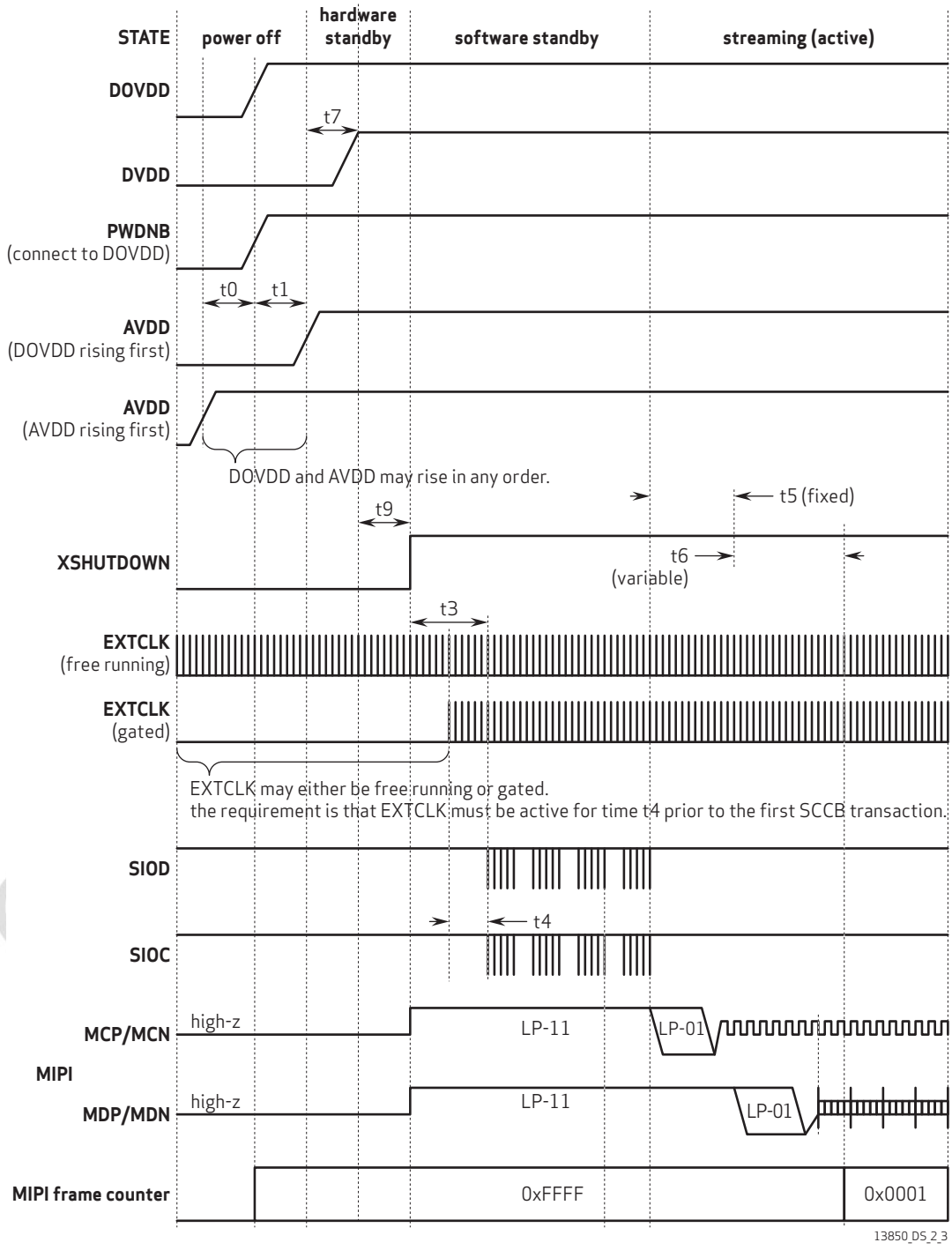
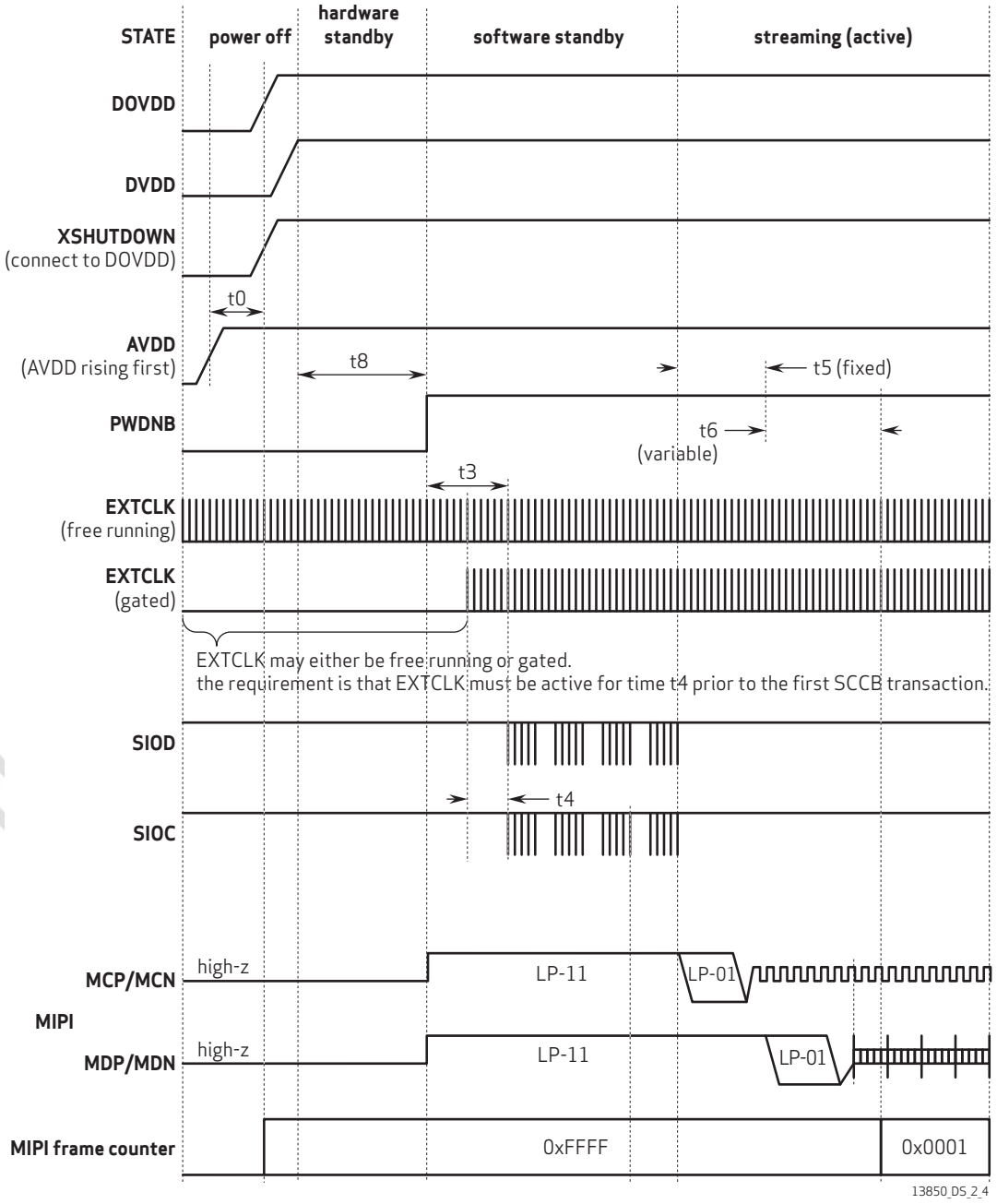


figure 2-4 power up sequence (case 2)



2.6.2 power down sequence

Similar to the power up sequence, the EXTCLK input clock may be either gated or continuous. If the SCCB command to exit streaming is received while a frame of MIPI data is being output, then the sensor must wait to the MIPI frame end code before entering software standby mode.

If the SCCB command to exit streaming mode is received during the inter frame time, then the sensor must enter software standby mode immediately.

Power down cases 1~2 corresponds to power up sequences 1~2, respectively.

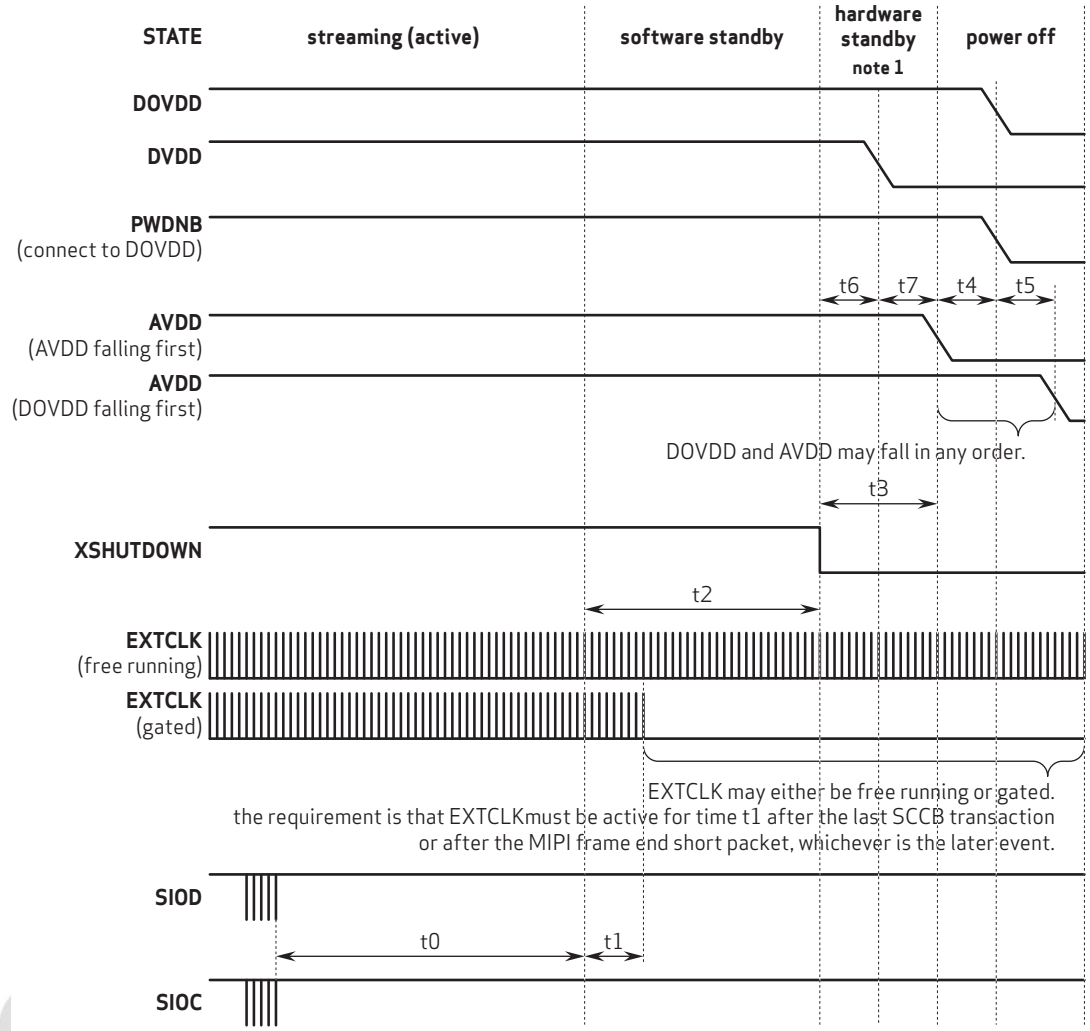
table 2-6 power down sequence

case	XSHUTDOWN	PWDNB	power down sequence requirement
1	GPIO	DOVDD	Refer to **figure 2-5** 1. software standby recommended 2. pull XSHUTDOWN low for low power consumption 3. cut off DVDD, then it will be in hardware standby state for minimum power consumption 4. pull AVDD and DOVDD low in any order
2	DOVDD	GPIO	Refer to **figure 2-6** 1. software standby recommended 2. pull PWDNB low for low power consumption 3. cut off DVDD, then it will be in hardware standby mode for minimum power consumption 4. turn off DOVDD 5. turn off AVDD

table 2-7 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for the MIPI end code before entering the software for standby; otherwise, enter the software standby mode immediately		
minimum of EXTCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		EXTCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDOWN falling	t2	512		EXTCLK cycles
XSHUTDOWN falling – AVDD falling or DOVDD falling whichever is first	t3	0.0		ns
AVDD falling – DOVDD falling	t4	AVDD and DOVDD may fall in any order, the falling separation can vary from 0 ns to infinity		ns
DOVDD falling – AVDD falling	t5			ns
XSHUTDOWN falling – external DVDD falling	t6	0.0		ns
external DVDD falling – AVDD falling or DOVDD falling whichever is first	t7	0.0		ns
PWDNB falling – external DVDD falling	t8	0.0		ns

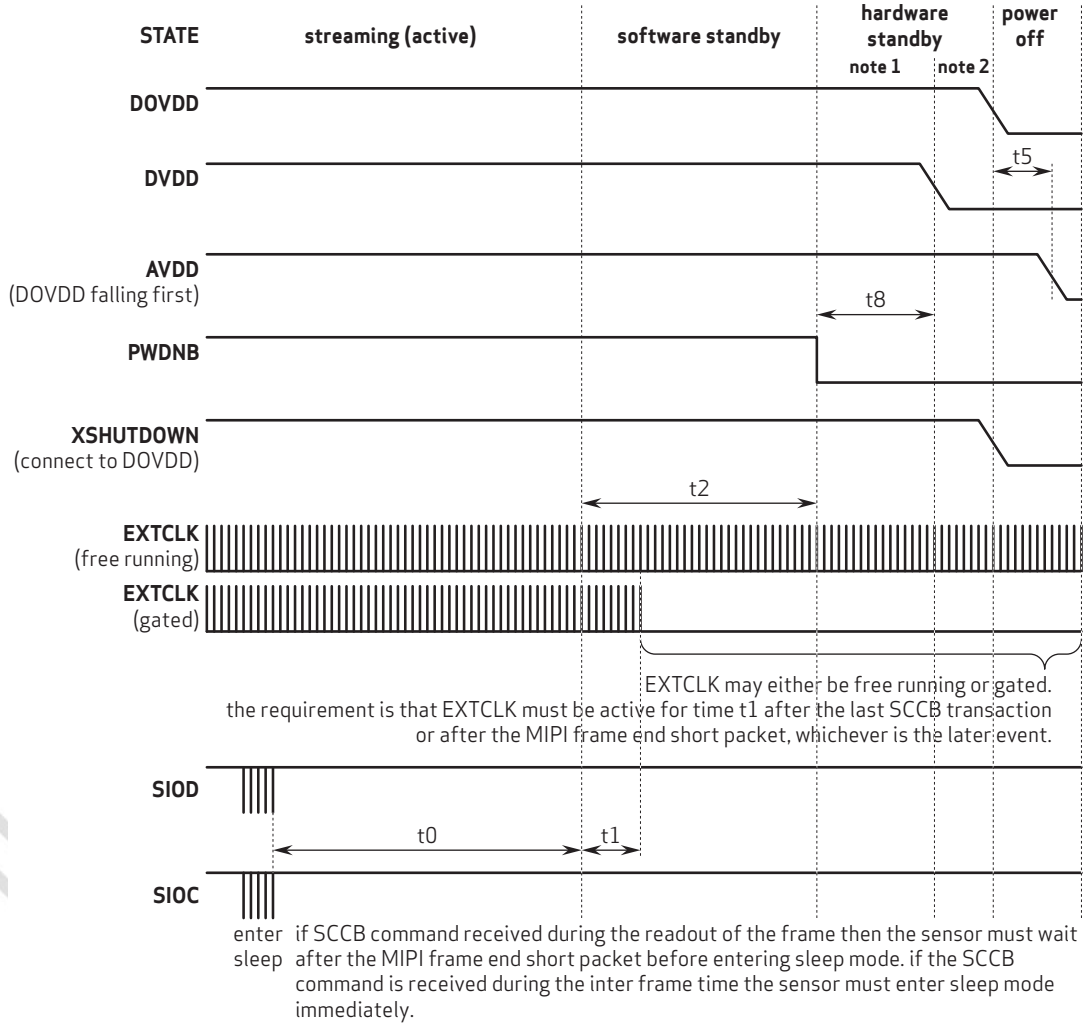
figure 2-5 power down sequence (case 1)



note 1 with minimum power consumption

13850_DS_2_5

figure 2-6 power down sequence (case 2)



note 1 with low power consumption

note 2 with minimum power consumption

13850_DS_2_6

2.7 reset

The OV13850 sensor includes a **XSHUTDOWN** pad (pad **46**) that forces a complete hardware reset when it is pulled low (GND). The OV13850 clears all registers and resets them to their default values when a hardware reset occurs. Reset requires ~2ms settling time.

2.7.1 power ON reset generation

The power on reset can be controlled from XSHUTDOWN pin. Additionally, inside this chip, a power on reset is generated after core power becomes stable.

2.8 hardware and software standby

Two suspend modes are available for the OV13850:

- **hardware standby**
- **software standby**

2.8.1 hardware standby

To initiate a hardware standby, the **PWDNB** pad (pad **47**) must be tied to low. When this occurs, the OV13850 internal device clock is halted and all internal counters are reset and register values are maintained.

2.8.2 software standby

Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

figure 2-7 standby timing (case 1)

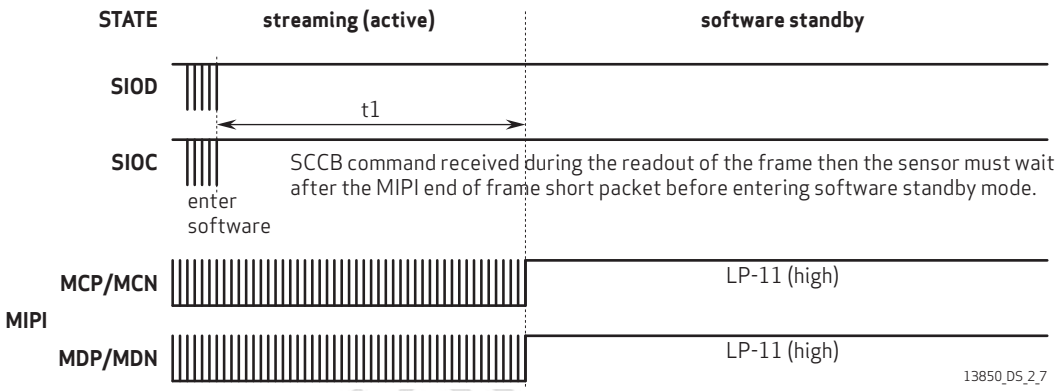
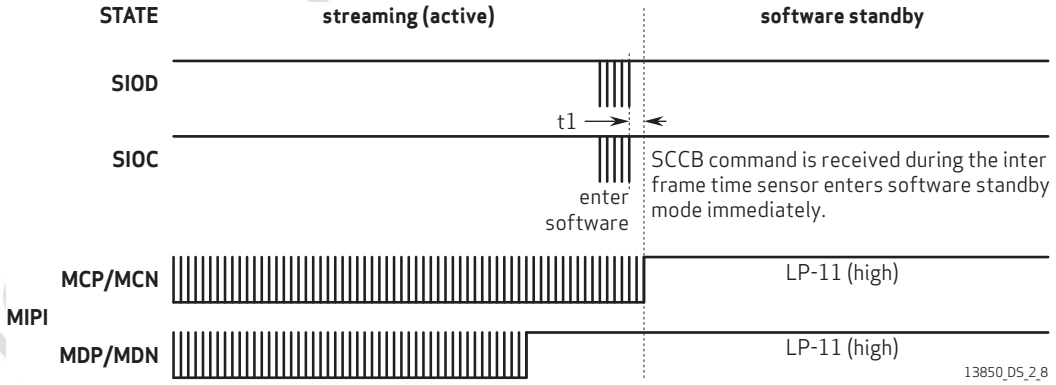


figure 2-8 standby timing (case 2)

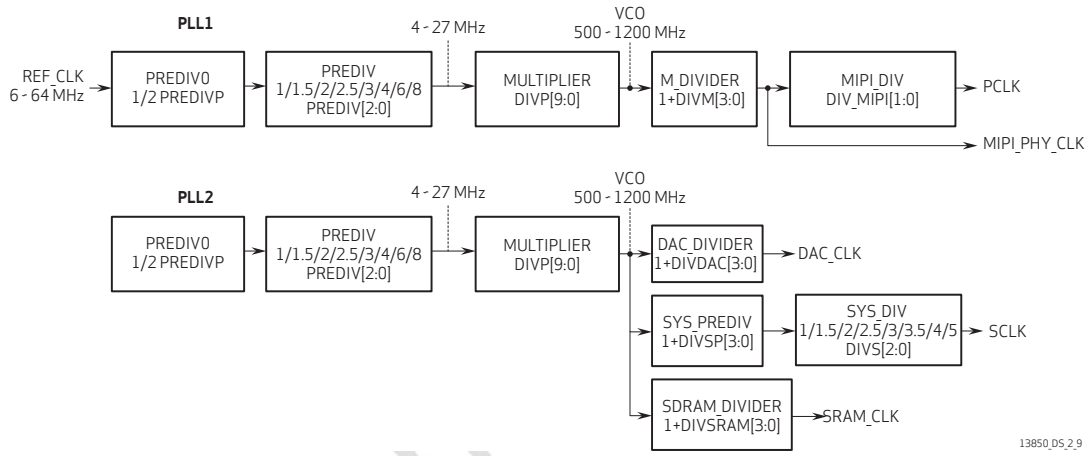


2.9 system clock control

The OV13850 has two on-chip PLLs which generate the system clock from a 6~64 MHz input clock. A programmable clock divider is provided to generate different frequencies for the system.

2.9.1 PLL configuration

figure 2-9 OV13850 PLL diagram



note
Contact your local OmniVision FAE for additional assistance on PLL configuration.

table 2-8 PLL1 registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x0300	PLL1_CTRL_0	0x00	RW	Bit[2:0]: PLL1_PREDIV 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0301	PLL1_CTRL_1	0x00	RW	Bit[1:0]: PLL1_DIVP[9:8]
0x0302	PLL1_CTRL_2	0x2A	RW	Bit[7:0]: PLL1_DIVP[7:0]

table 2-8 PLL1 registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x0303	PLL1_CTRL_3	0x00	RW	Bit[3:0]: PLL1_DIVM 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16
0x0304	PLL1_CTRL_4	0x03	RW	Bit[1:0]: PLL1_DIV_MIPI 00: /4 01: /5 10: /6 11: /8
0x0305	PLL1_CTRL_5	0x01	RW	Bit[1:0]: PLL1_DIV_SP 00: /3 01: /4 10: /5 11: /6
0x0306	PLL1_CTRL_6	0x01	RW	Bit[0]: PLL1_DIV_S 0: /1 1: /2
0x0308	PLL1_CTRL_8	0x00	RW	Bit[0]: PLL1_bypass
0x0309	PLL1_CTRL_9	0x01	RW	Bit[2:0]: PLL1_CP
0x030A	PLL1_CTRL_A	0x00	RW	Bit[0]: PLL1_PREDIVP 0: /1 1: /2

table 2-9 PLL2 registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3611	ASP_CTRL17	0x10	RW	Bit[7]: PLL2_bypass 0: Working 1: Bypass Bit[6:4]: PLL2_CP Default 001 Bit[3]: PLL2_PREDIVP 0: By 1 1: By 2 Bit[2:0]: PLL2_PREDIV 000: 1 001: 1.5 010: 2 011: 2.5 100: 3 101: 4 110: 6 111: 8
0x3612	ASP_CTRL18	0x23	RW	Bit[7]: Power down PUMP clock divider 0: Working 1: Power down Bit[6:4]: PLL2_DIVS System clock divider control bits 000: 1 001: 1.5 010: 2 011: 2.5 100: 3 101: 3.5 110: 4 111: 5 Bit[3:0]: PLL2_DIVSP System clock pre_divider control bit value = [3:0] + 1
0x3613	ASP_CTRL19	0x33	RW	Bit[7:4]: PLL2_DIVSRAM SRAM clock divider control bit Value=[3:0]+1 Bit[3:0]: PLL2_DIVDAC DAC clock divider control bit value = [3:0] + 1
0x3614	ASP_CTRL20	0x28	RW	Bit[7:0]: PLL2_DIVP[7:0] Loop divider control value = [9:0]

table 2-9 PLL2 registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3615	ASP_CTRL21	0x1C	RW	Bit[5:4]: N_PUMP clock div[1:0] Div number 00: /2 01: /3 10: /4 11: /8 Bit[3:2]: P_PUMP clock div[1:0] Div number 00: /2 01: /3 10: /4 11: /8 Bit[1:0]: PLL2_DIVP[9:8]

table 2-10 sample PLL configuration (sheet 1 of 2)

name	address	input clock (EXTCLK)			
		24 MHz	27 MHz	13.33 MHZ	6 MHz
PLL1_PREDIV	0x0300	0x00	0x01	0x00	0x00
PLL1_DIVP_H	0x0301	0x00	0x00	0x00	0x00
PLL1_DIVP_L	0x0302	0x32	0x43	0x5A	0xC8
PLL1_DIVM	0x0303	0x00	0x00	0x00	0x00
PLL1_DIV_MIPI	0x0304	0x03	0x03	0x03	0x03
PLL1_PREDIVP	0x030A	0x00	0x00	0x00	0x00
PLL2_PREDIVP	0x3611[3]	0x00	0x00	0x00	0x00
PLL2_PREDIV	0x3611[2:0]	0x00	0x01	0x00	0x00
PLL2_DIV_SYS	0x3612[6:4]	0x02	0x02	0x02	0x02
PLL2_DIV_SYS_SP	0x3612[3:0]	0x03	0x03	0x03	0x03
PLL2_DIV_SRAM	0x3613[7:4]	0x03	0x03	0x03	0x03
PLL2_DIV_DAC	0x3613[3:0]	0x03	0x03	0x03	0x03
PLL2_DIVP_L	0x3614[7:0]	0x28	0x36	0x48	0xA0
PLL2_DIVP_H	0x3615[1:0]	0x00	0x00	0x00	0x00
HTS high byte	0x380C	0x12	0x12	0x12	0x12
HTS low byte	0x380D	0xC0	0xC0	0xC0	0xC0

table 2-10 sample PLL configuration (sheet 2 of 2)

name	address	input clock (EXTCLK)			
		24 MHz	27 MHz	13.33 MHZ	6 MHz
VTS high byte	0x380E	0x0D	0x0D	0x0D	0x0D
VTS low byte	0x380F	0x00	0x00	0x00	0x00
SCLK		120 MHz	121.5 MHz	119.97 MHz	120 MHz
DAC_CLK		240 MHz	243 MHz	239.94 MHz	240 MHz
MIPI_SCLK		1200 MHz	1206 MHz	1199.7 MHz	1200 MHz
MIPI_PCLK		150 MHz	150.75 MHz	149.96 MHz	150 MHz

table 2-11 PLL speed limitation

parameter	value
PLL1_multiplier input	4~27 MHz
PLL1_multiplier output	500~1200 MHz
PLL2_multiplier input	4~27 MHz
PLL2_multiplier output	500~1200 MHz
SCLK	max 126 MHz
REF_CLK	6~64 MHz

2.10 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

In the OV13850, the SCCB ID is controlled by the SID pin, and can be programmable. If SID is low, the sensor's SCCB address comes from register 0x300C which has a default value of 0x20. If SID is high, the sensor's SCCB address comes from register 0x3661 which has a default value of 0x6C.

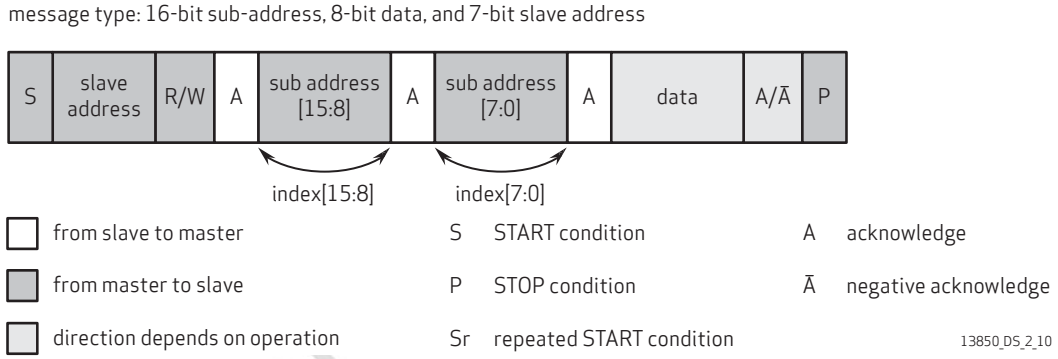
2.10.1 data transfer protocol

Data transfer of the OV13850 follows the SCCB protocol.

2.10.2 message format

The OV13850 supports the message format shown in **figure 2-10**. The repeated START (Sr) condition is not shown in **figure 2-10**, but is shown in **figure 2-11** and **figure 2-13**.

figure 2-10 message type



2.10.3 read / write operation

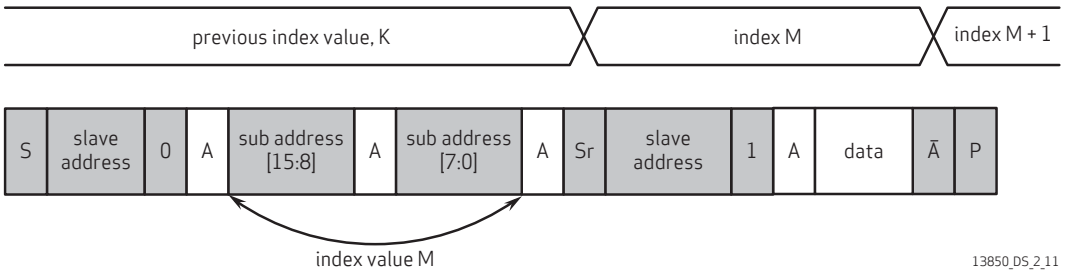
The OV13850 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

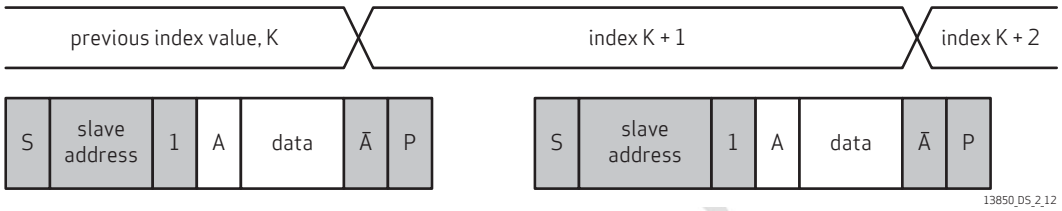
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SIOD line as shown in **figure 2-11**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-11 SCCB single read from random location



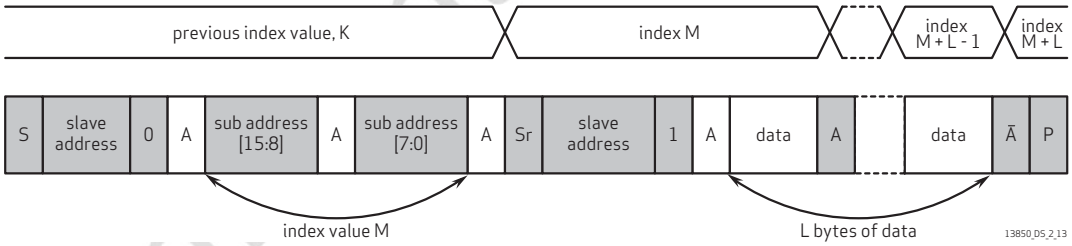
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SIOD line as shown in **figure 2-12**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-12 SCCB single read from current location



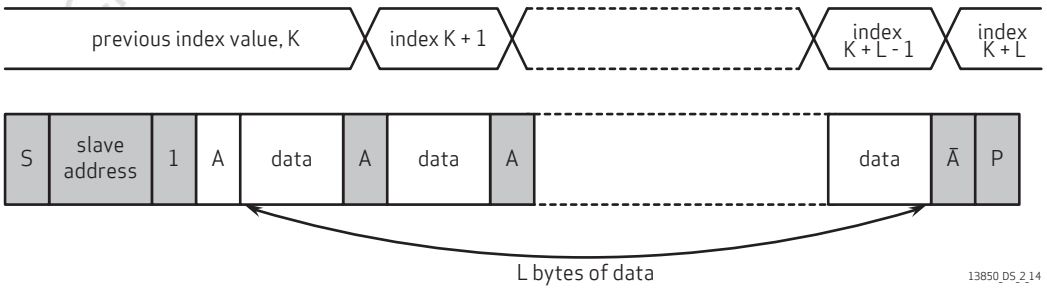
The sequential read from a random location is illustrated in **figure 2-13**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-13 SCCB sequential read from random location



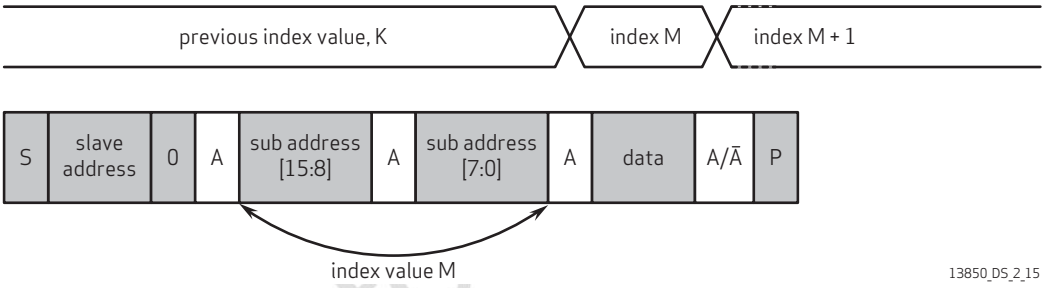
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation. as shown in **figure 2-14**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-14 SCCB sequential read from current location



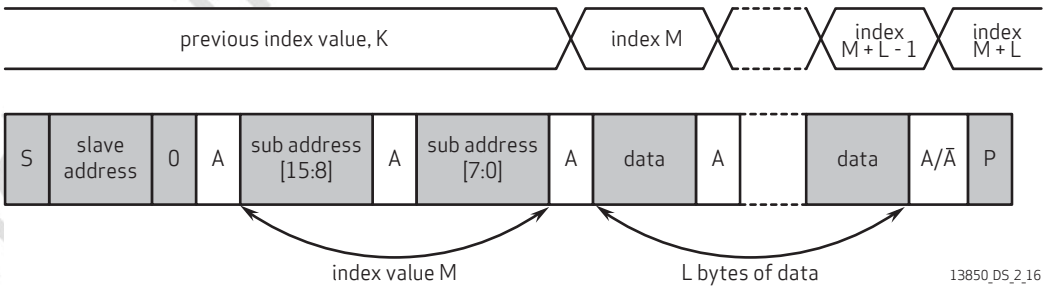
The write operation to a random location is illustrated in **figure 2-15**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-15 SCCB single write to random location



The sequential write is illustrated in **figure 2-16**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-16 SCCB sequential write to random location



2.10.4 SCCB timing

figure 2-17 SCCB interface timing

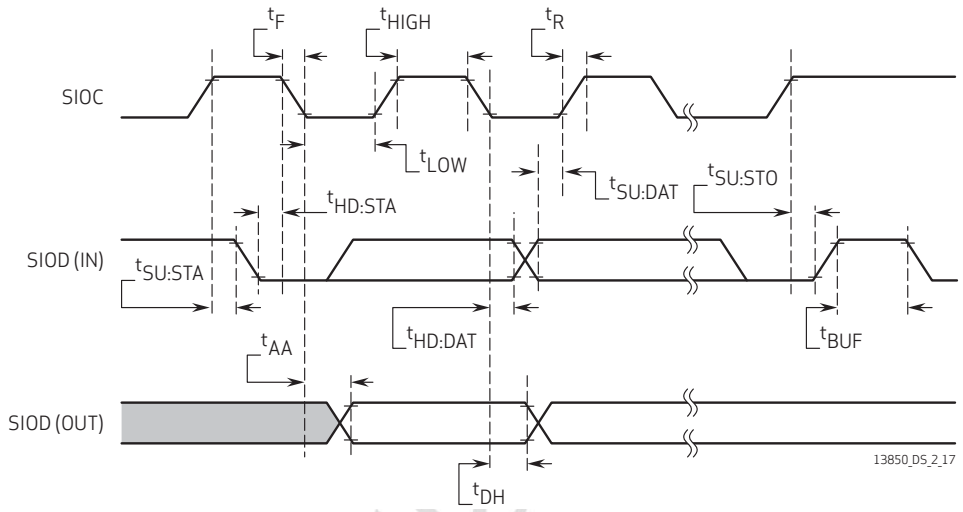


table 2-12 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SIOC}	clock frequency	TBD	TBD	TBD	kHz
t_{LOW}	clock low period	TBD	TBD	TBD	µs
t_{HIGH}	clock high period	TBD	TBD	TBD	µs
t_{AA}	SIOC low to data out valid	TBD	TBD	TBD	µs
t_{BUF}	bus free time before new start	TBD	TBD	TBD	µs
$t_{HD:STA}$	start condition hold time	TBD	TBD	TBD	µs
$t_{SU:STA}$	start condition setup time	TBD	TBD	TBD	µs
$t_{HD:DAT}$	data in hold time	TBD	TBD	TBD	µs
$t_{SU:DAT}$	data in setup time	TBD	TBD	TBD	µs
$t_{SU:STO}$	stop condition setup time	TBD	TBD	TBD	µs
t_R, t_F	SCCB rise/fall times	TBD	TBD	TBD	µs
t_{DH}	data out hold time	TBD	TBD	TBD	µs

a. SCCB timing is based on 1MHz and 400kHz modes

b. timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 30%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 70%

2.10.5 group write

The OV13850 supports four groups. These groups share 1024x8 bits or 1024 bytes and the size of each group is programmable by adjusting the start address.

Group write is supported in order to update a group of registers in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary.

table 2-13 context switching control

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Group Access Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 0110: Group launch at line blank 1010: Group launch at vertical blank 1110: Group launch immediately Others: Reserved Bit[3:0]: group_id 0000: Group bank 0, default start from address 0x00 0001: Group bank 1, default start from address 0x40 0010: Group bank 2, default start from address 0x80 0011: Group bank 3, default start from address 0xB0 Others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	Number of Frames to Stay in Group 0
0x320A	GRP1_PERIOD	0x00	RW	Number of Frames to Stay in Group 1
0x320B	GRP_SWCTRL	0x01	RW	Bit[4]: frame_cnt_trig Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: Second group selection
0x320D	GRP_ACT	–	R	Indicates Which Group is Active
0x320E	FRAME_CNT_GRP0	–	R	frame_cnt_grp0
0x320F	FRAME_CNT_GRP1	–	R	frame_cnt_grp1

2.11 hold

After the groups are configured, users can perform a hold operation to store register settings into the SRAM of each group. The hold of each group starts and ends with control register 0x3208. The lower 4 bits of register 0x3208 control which group to access, and the upper 4 bits control the start (0x0: hold start) and end (0x1: hold end) of the hold operation.

The example setting below shows the sequence to hold group 0:

```
20  3208  00    group 0 hold start
20  3800  11    first register into group 0
20  3911  22    second register into group 0
20  3208  10    group 0 hold end
```

2.12 launch

After the contents of each group are defined in the hold operation, all registers belonging to each group are stored in SRAM and ready to be written into target registers (i.e., the launch of that group).

There are five launch modes as described in **section 2.12.1** to **section 2.12.5**.

2.12.1 launch mode 1 - quick manual launch

Manual launch is enabled by setting register 0x320B to 0.

Quick manual launch is achieved by writing to control register 0x3208. The value written into this register is 0xEX, the upper 4 bits (0xE) are the quick launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 0, they just write the value 0xE0 to register 0x3208, then the contents of group 0 will be written to the target registers immediately after the sensor gets this command through the SCCB. Below is an example of this setting.

```
20  320B  00    manual launch on
20  3208  E0    quick launch group 0
```

2.12.2 launch mode 2 - delay manual launch

Delay manual launch is achieved by writing to register 0x3208. The value written into this register is 0xAX, where the upper 4 bits (0xA) are the delay launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 1, they just write the value 0xA1 to register 0x3208, then the contents of group 1 will be written to the target registers. The difference with mode 1 is that the writing will wait for some internally defined time spot in vertical blanking; thus delayed. Below is an example of this setting.

```
20  320B  00    manual launch on
20  3208  A1    delay launch group 1
```

2.12.3 launch mode 3 - quick auto launch

Quick auto launch works like the mode 1, but the difference is it will return to a specified group automatically. This is controlled by the register 0x3209, where bit[6:5] controls which group to return and bit[4:0] controls how many frames to stay before returning. The auto launch enable bit is the 0x320B[7]. The operation can be better understood with an example of this setting:

```
20  3209  44    Bit[6:5]: 2, return to group 2, Bit[4:0]: 4: stay 4 frames
20  320B  80    auto launch on
20  3208  E0    quick launch group 0
```

In this example, the sensor will quick launch group 0, stay at group 0 for 4 frames, and then return to group 2.

2.12.4 launch mode 4: delay auto launch

Delay auto launch works like mode 2 in the delay launch part and like the mode 3 in the return part.

The operation can be better understood with an example of this setting:

```
20  3209  44    Bit[6:5]: 2, return to group 2, Bit[4:0]: 4: stay 4 frames
20  320B  80    auto launch on
20  3208  A0    delay launch group 0
```

In this example, the sensor will delay launch group 0, stay at group 0 for 4 frames, and then return to group 2.

2.12.5 launch mode 5: repeat launch

Repeat launch is controlled by registers 0x3209, 0x320A, and 0x320B. In this mode, the launch is repeated automatically between the first group (must be group 0) and the second group (can be either one of groups 1-3, which is specified by register 0x320B[1:0]). Register 0x3209 defines how many frames remain in group 0 and register 0x320A defines how many frames remain in the second group.

The operation can be better understood with an example of this setting:

```
20  3209  02    Bit[7:0]: 2, stay 2 frames in group 0
20  320A  03    Bit[7]: 3, stay 3 frames in the second group
20  320B  0E    Bit[3:2]: 3, repeat launch on, Bit[1:0]: 2, second group select:
                group 2
20  3208  A0    always use a0 for repeat launch
```

In this example, the sensor will delay launch group 0, stay at group 0 for 2 frames, then switch to group 2 for 3 frames, then back to group 0 for 2 frames, group 2 for 3 frames and so on.

Below is another example that shows applying launch mode 2 (delay manual launch) first, the sensor stays at group 2 for an indefinite number of frames, and then applying launch mode 5 (repeat launch). The sensor will switch to group 0 for 2 frames, then group 2 for 3 frames, and so on.

```
20  320B  00    manual launch on
20  3208  A2    delay launch group 2 stay at group 2 for indefinite frames
20  3209  02    Bit[7:0]: 2, stay 2 frames in group 0
20  320A  03    Bit[7:0]: 3, stay 3 frames in the second group
20  320B  0E    Bit3:2]: 3, repeat launch on, Bit[1:0]: 2, second group select:
                group 2
20  3208  A0    always use A0 for repeat launch
```

Switch to group 0 for 2 frames, then group 2 for 3 frames, and so on.

3 block level description

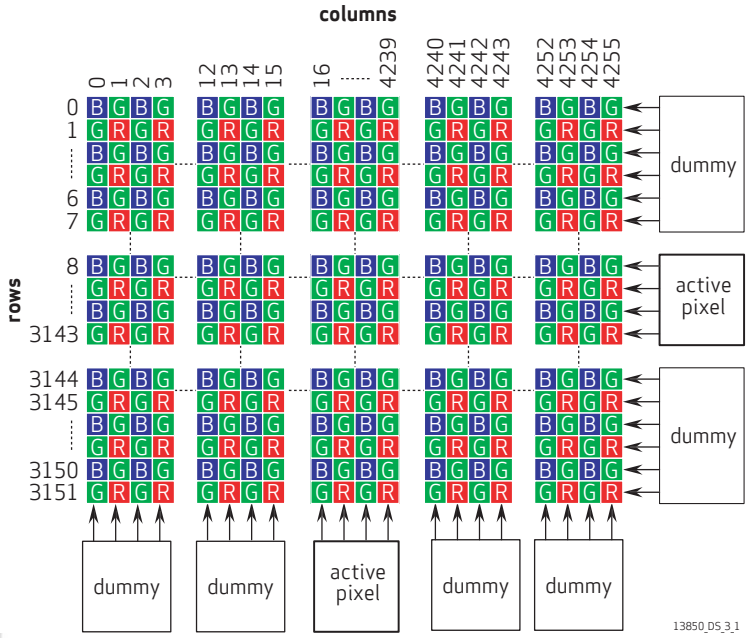
3.1 pixel array structure

The OV13850 sensor has an image array of 4256 columns by 3152 rows (13,414,912 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 13,414,912 pixels, 13,246,464 (4224x3136) are active pixels and can be output.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout



3.2 subsampling

Binning mode is usually used for low resolution. When the binning function is ON, voltage levels of adjacent pixels are averaged. If the binning function is OFF, the pixels, which are not output, are merely skipped. The OV13850 supports 2x2 binning. In **figure 3-2**, the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged before entering the ADC.

figure 3-2 example of 2x2 binning

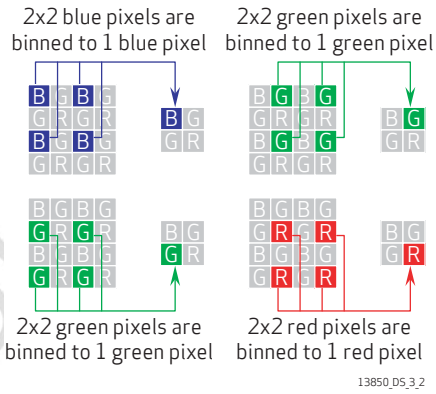


table 3-1 binning-related registers

address	register name	default value	R/W	description
0x3820	TIMING_FORMAT1	0x00	RW	Bit[0]: Vertical binning
0x3821	TIMING_FORMAT2	0x00	RW	Bit[0]: Horizontal binning

3.3 alternate row HDR

In HDR mode, the exposure is still controlled by a rolling shutter. However, the frame data is separated into "long exposure" and "short exposure" in every two rows, as shown in **figure 3-3**. Long exposure time is controlled by registers 0x3500, 0x3501, and 0x3502. Short exposure time is controlled by registers 0x3506, 0x3507, and 0x3508. The sequence of MIPI output in HDR mode is similar to normal mode. The output timing of long and short exposure lines is shown in **figure 3-4**

figure 3-3 alternate row HDR

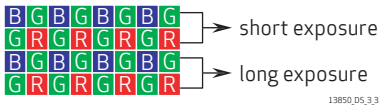


figure 3-4 HDR output timing

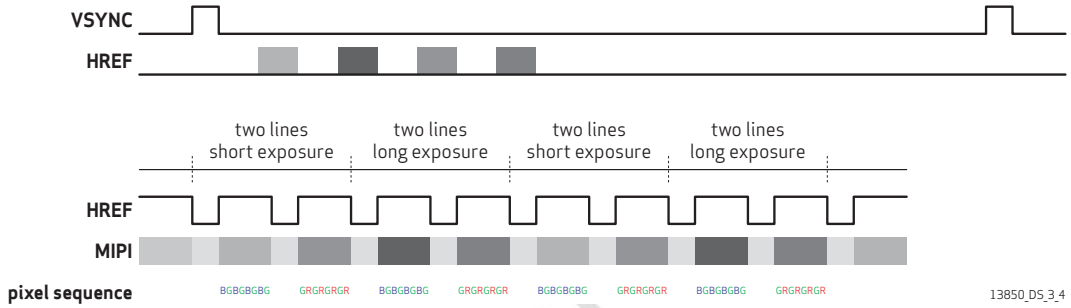


table 3-2 HDR control registers

address	register name	default value	R/W	description
0x3821	TIMING_FORMAT2	0x08	RW	HDR Enable Bit[7]: hdr_en 0: Disable 1: Enable
0x3500	MEC LONG EXPO	0x00	RW	Long Exposure Bit[7:4]: Not used Bit[3:0]: Long exposure[19:16]
0x3501	MEC LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[15:8]
0x3502	MEC LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0
0x3506	MEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:4]: Not used Bit[3:0]: Short exposure[19:16]
0x3507	MEC SHORT EXPO	0x02	RW	Short Exposure Bit[7:0]: Short exposure[15:8]
0x3508	MEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0

4 image sensor core digital functions

4.1 mirror and flip

The OV13850 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

13850_DS_4_1

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	TIMING_REG20	0x00	RW	Timing Control Register Bit[2]: Vertical flip enable 0: Normal 1: Vertical flip
0x3821	TIMING_REG21	0x00	RW	Timing Control Register Bit[2]: Horizontal mirror enable 0: Normal 1: Horizontal mirror

4.2 image cropping and windowing

An image windowing area is defined by four parameters, horizontal start (HS), horizontal end (HE), vertical start (VS), and vertical end (VE). By properly setting the parameters, any portion within the sensor array can be output as a visible area. Windowing is achieved by simply masking off the pixels outside the window; thus, the timing is not affected.

figure 4-2 image cropping and windowing

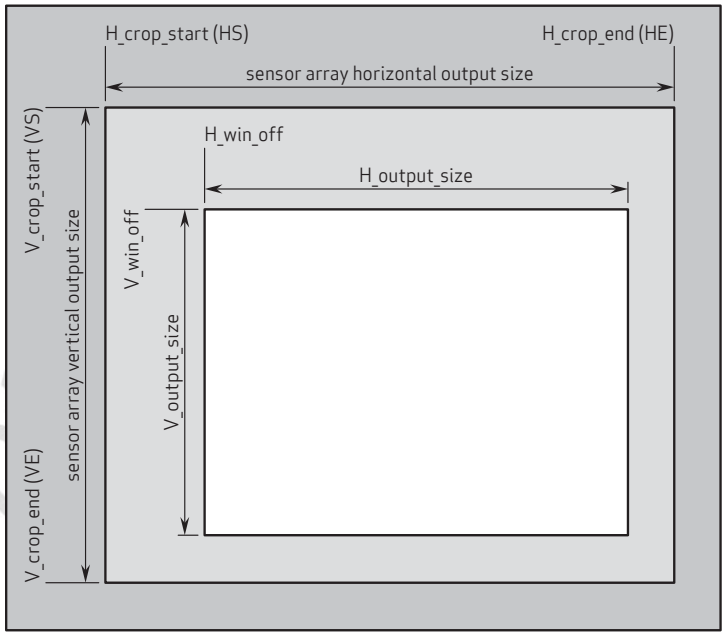


table 4-2 image cropping and windowing control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	H_CROP_START	0x00	RW	Bit[4:0]: Horizontal crop start address[12:8]
0x3801	H_CROP_START	0x14	RW	Bit[7:0]: Horizontal crop start address[7:0]
0x3802	V_CROP_START	0x00	RW	Bit[3:0]: Vertical crop start address[11:8]
0x3803	V_CROP_START	0x0C	RW	Bit[7:0]: Vertical crop start address[7:0]
0x3804	H_CROP_END	0x10	RW	Bit[4:0]: Horizontal crop end address[12:8]
0x3805	H_CROP_END	0x8B	RW	Bit[7:0]: Horizontal crop end address[7:0]
0x3806	V_CROP_END	0x0C	RW	Bit[3:0]: Vertical crop end address[11:8]

table 4-2 image cropping and windowing control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3807	V_CROP_END	0x43	RW	Bit[7:0]: Vertical crop end address[7:0]
0x3808	H_OURPUT_SIZE	0x10	RW	Bit[4:0]: Horizontal output size[12:8]
0x3809	H_OUTPUT_SIZE	0x70	RW	Bit[7:0]: Horizontal output size[7:0]
0x380A	V_OURPUT_SIZE	0x0C	RW	Bit[3:0]: Vertical output size[11:8]
0x380B	V_OUTPUT_SIZE	0x30	RW	Bit[7:0]: Vertical output size[7:0]
0x380C	TIMING_HTS	0x12	RW	Bit[6:0]: Horizontal total size[14:8]
0x380D	TIMING_HTS	0xC0	RW	Bit[7:0]: Horizontal total size[7:0]
0x380E	TIMING_VTS	0x0D	RW	Bit[6:0]: Vertical total size[14:8]
0x380F	TIMING_VTS	0x00	RW	Bit[7:0]: Vertical total size[7:0]
0x3810	H_WIN_OFF	0x00	RW	Bit[3:0]: Horizontal windowing offset[11:8]
0x3811	H_WIN_OFF	0x04	RW	Bit[7:0]: Horizontal windowing offset[7:0]
0x3812	V_WIN_OFF	0x00	RW	Bit[3:0]: Vertical windowing offset[11:8]
0x3813	V_WIN_OFF	0x04	RW	Bit[7:0]: Vertical windowing offset[7:0]
0x3814	H_INC	0x11	RW	Bit[7:4]: Horizontal sub-sample odd increase number Bit[3:0]: Horizontal sub-sample even increase number
0x3815	V_INC	0x11	RW	Bit[7:4]: Vertical sub-sample odd increase number Bit[3:0]: Vertical sub-sample even increase number

4.3 test pattern

For testing purposes, there are four types of test patterns. The two types of digital test patterns are color bar and random data. The OV13850 also offers two digital effects: transparent effect and rolling bar effect. The output type of digital test pattern is controlled by the test_pattern_type register (0x5E00[3:2]). The digital test pattern function is controlled by register 0x5E00[7].

4.3.1 color bar

There are four types of color bars which are switched by bar-style in register 0x5E00[3:2] (see **figure 4-3**).

figure 4-3 color bar types

13850_DS_4_3

4.3.2 random data

There are two types of random data test patterns: frame-changing and frame-fixed random data.

4.3.3 transparent effect

The transparent effect is enabled by transparent_en register (0x5E00[5]). If this register is set, the transparent test pattern will be displayed. **figure 4-4** is an example showing a transparent color bar image.

figure 4-4 transparent effect

1138505_DS_4.4

4.3.4 rolling bar effect

The rolling bar is set by rolling_bar_en register (0x5E00[6]). If it is set, an inverted color rolling bar will roll from top to bottom. **figure 4-5** is an example showing a rolling bar on a color bar image.

figure 4-5 rolling bar effect

13850_DS_4.5

4.4 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration.

There are two main functions of the BLC:

- applying all normal pixel values based on the values of the black levels
- applying multiplication to all the pixel values based on digital gain

table 4-3 BLC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5001	R ISP CTRL1	0x01	RW	Bit[0]: BLC_en

table 4-3 BLC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0xF1	RW	Bit[7]: outrange_trig_en Offset out of range trigger function enable signal 0: Disable 1: Enable Bit[6]: format_chg_en Format change trigger function enable signal 0: Disable 1: Enable Bit[5]: gain_chg_en Gain change trigger function enable signal 0: Disable 1: Enable Bit[4]: Not used Bit[3]: manual_trig Manual trigger signal Its rising edge will trigger BLC Bit[2]: freeze_en BLC freeze function enable signal When it is set, the BLC will be frozen. Offsets will keep the their pre-frame values. Bit[1]: always_do BLC always trigger signal When it is set, the BLC will be triggered every frame unless the freeze_en is enabled. Bit[0]: median_en 5-point median filter function enable signal 0: Disable 1: Enable
0x4001	BLC CTRL01	0x00	RW	Bit[1]: blc_cut_range_en Bit[0]: remove_row_offset_en Column delta offset remove function enable signal 0: Used offset does not include column delta offset 1: Used offset includes column delta offset
0x4004	TARGET	0x00	RW	Bit[7:0]: Target[15:8]
0x4005	TARGET	0x10	RW	Bit[7:0]: Target[7:0]
0x4006	BLC CTRL 06	0x1F	RW	Bit[7:0]: format_trig_framenumber
0x4007	BLC CTRL 07	0x1F	RW	Bit[7:0]: reset_trig_framenumber

table 4-3 BLC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x4008	BLC CTRL 08	0x01	RW	Bit[7:0]: manual_trig_framenumber
0x400C	OFFSET TRIG THRESH	0x00	RW	Bit[7:0]: offset_trig_thresh[15:8]
0x400D	OFFSET TRIG THRESH	0x20	RW	Bit[7:0]: offset_trig_thresh[7:0]

4.5 one time programmable (OTP) memory

The OV13850 supports a maximum of 1024 bytes of one-time programmable (OTP) memory to store chip identification and manufacturing information, which can be used to update the sensor's default setting and can be controlled through the SCCB (see **table 4-4**).

4.5.1 OTP other functions

OTP loading data can be triggered when power up or writing 0x01 to register 0x3D81. Power up loading data is controlled by register 0x3D85[2], and by default is off. Auto mode and manual mode can be chosen by setting register 0x3D84[6] to 0 and 1, respectively, and by default, it is in auto mode. In auto mode, all data in the OTP will be loaded to the OTP buffer, while in manual mode, part of the data, which is defined by the start address ({0x3D88, 0x3D89}) and the end address ({0x3D8A, 0x3D8B}) of the OTP, will be loaded to the OTP buffer.

The OTP memory access conditions are based on typical conditions: sensor wakeup, 2.8~3.0V AVDD, 1.2V DVDD, and 120 MHz system clock.

OTP access requires special timing. In order for OTP access to work with default settings, SCLK should be between 68~126 MHz.

To use OTP memory under different operating conditions, please contact your local OmniVision FAE.

table 4-4 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x7000~ 0x73FF	OTP_SRAM	0x00	RW	Bit[7:0]: OTP buffer
0x3D80	OTP_PROGRAM_CTRL	0x00	RW	Bit[7]: OTP_wr_busy Bit[0]: OTP_program_enable
0x3D81	OTP_LOAD_CTRL	0x00	RW	Bit[7]: OTP_rd_busy Bit[0]: OTP_load_enable

table 4-4 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D84	OTP_MODE_CTRL	0x00	RW	Bit[7]: Program disable 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode
0x3D85	OTP_REG85	0x13	RW	Bit[2]: OTP power up load data enable Bit[1]: OTP power up load setting enable Bit[0]: OTP write register load setting enable
0x3D88	OTP_START_ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode
0x3D8A	OTP_END_ADDRESS	0x00	RW	OTP End High Address For Manual Mode
0x3D8B	OTP_END_ADDRESS	0x00	RW	OTP End Low Address For Manual Mode
0x3D8C	OTP_SETTING_STT_ADDRESS	0x00	RW	OTP Start High Address For Load Setting
0x3D8D	OTP_SETTING_STT_ADDRESS	0x00	RW	OTP Start Low Address For Load Setting

4.6 temperature sensor

The OV13850 supports an on-chip temperature sensor that covers -64 ~ +192°C with an average range of 5°C. It can be controlled through the SCCB interface (see **table 4-5**).

Before reading the temperature, the temperature sensor should be triggered by a 0 to 1 transition of register 0x4D12[0]. There is a 64°C offset in the readout value. The junction temperature can be calculated by converting the readout value from hex to decimal and subtracting 64.

table 4-5 temperature sensor functions

function	register	R/W	description
TPM trigger	0x4D12	RW	Bit[0]: Temperature sensor trigger
TPM read	0x4D13	R	Bit[7:0]: Temperature readout

4.7 strobe flash

4.7.1 strobe flash control

The strobe signal is programmable. It supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. The OV13850 supports the following flashlight modes (see **table 4-6**).

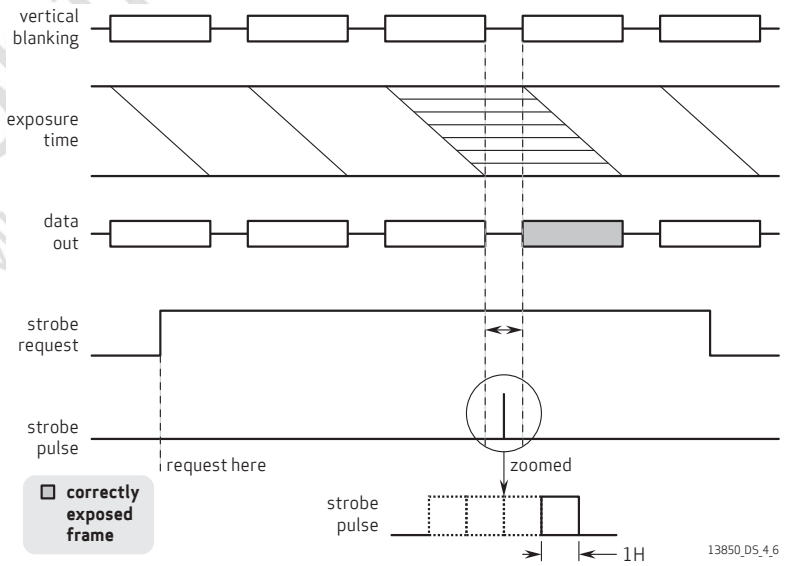
table 4-6 flashlight modes

mode	output	additional exposure lines
xenon	one-pulse	yes
LED 1	one-pulse	yes
LED 2	continuous	yes
LED3	continuous	no
LED4	one-pulse	yes

4.7.1.1 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see **figure 4-6**). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H, where H is one row period.

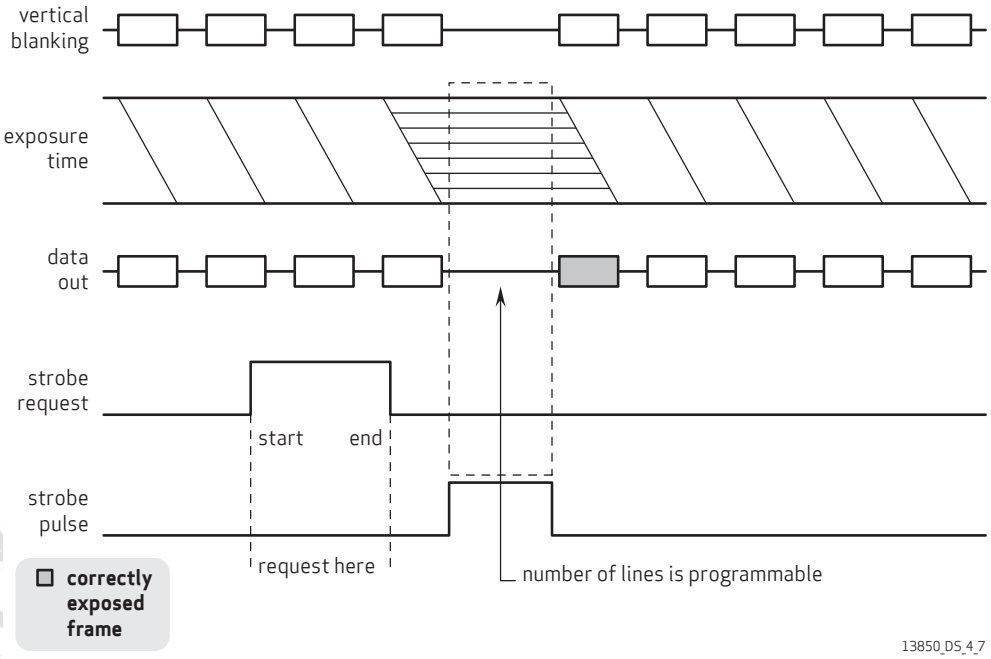
figure 4-6 xenon flash mode



4.7.1.2 LED 1 & 2 mode

In LED 1 & 2 modes, the strobe pulse is active two frames after the strobe request is submitted and the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set as shown in **figure 4-7**. If end request has not been sent, the strobe signal is activated intermittently until the strobe end request is set (see **figure 4-8**). The strobe width is programmable.

figure 4-7 LED 1 & 2 mode - one pulse output

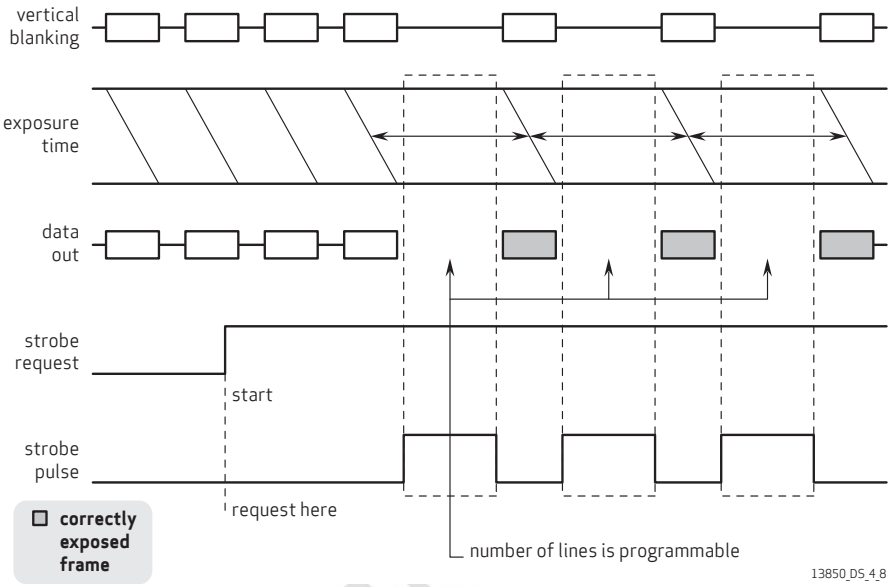


The strobe width is controlled by registers 0x3B02 and 0x3B03. The inserted dummy lines are used for the additional exposure lines added to 0x3500~0x3503. The maximum line of 0x3B02 and 0x3B03 is calculated by 0x7FFF0 - (0x3500, 0x3501, 0x3502).

Example of LED 1 & 2 mode:

```
20 3b00 01 ;Select led 1 mode
20 3b02 00 ;Set strobe width
20 3b03 3f ;Set strobe width
20 3002 80 ;Set the Vsync output enable
20 3b00 81 ;Request on
;delay 100 ;if using LED 2 mode
20 3b00 00 ;Request off
```

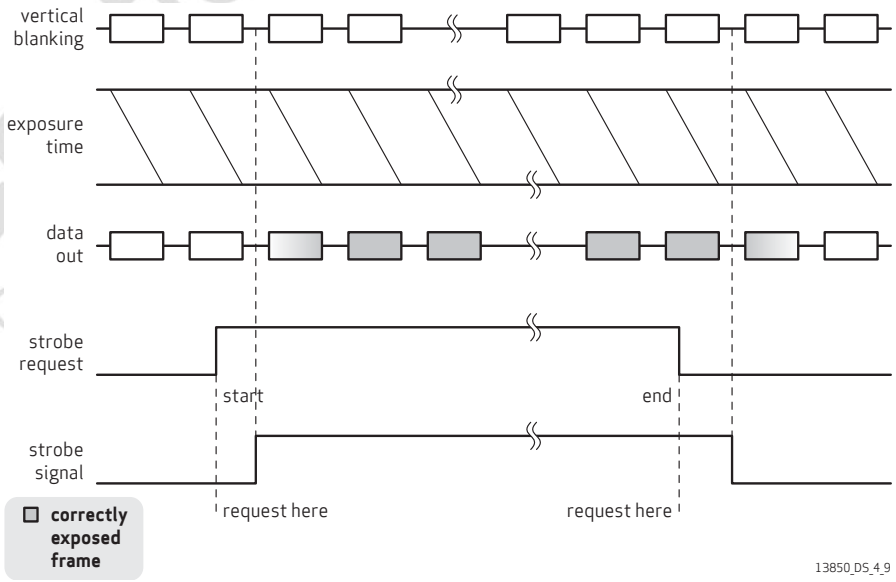
figure 4-8 LED 1 & 2 mode - multiple pulse output



4.7.1.3 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see figure 4-9).

figure 4-9 LED 3 mode



4.7.1.4 LED 4 mode

In LED 4 mode, the strobe signal width is controlled by register 0x3B05 (see **figure 4-10**). Strobe width = 128 × (2^0x3B05[1:0]) × (0x3B05[7:2] + 1) × sclk_period. The maximum value of 0x3B05[7:2] is 6'b111110.

figure 4-10 LED 4 mode

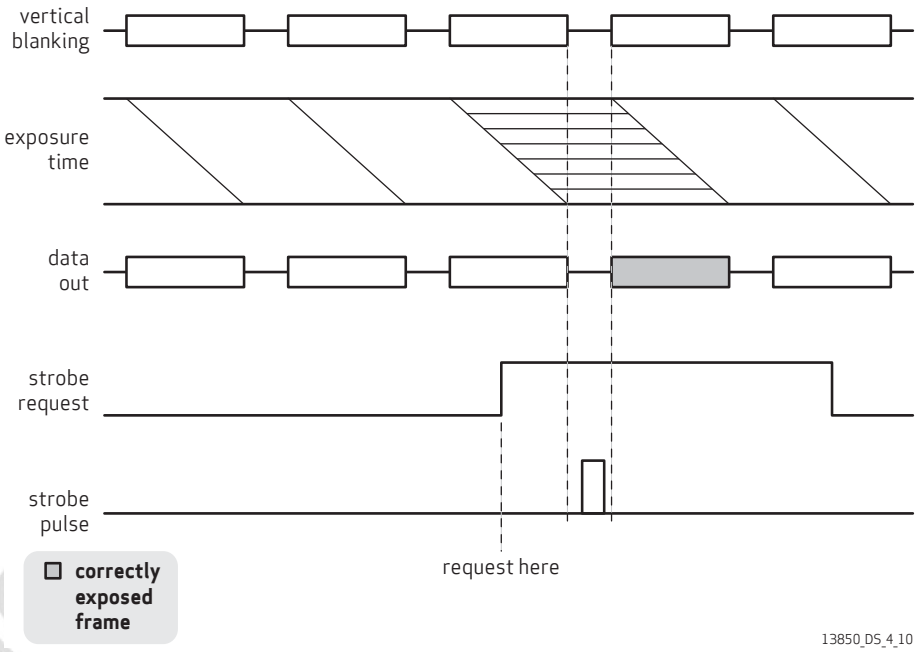


table 4-7 LED strobe control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE CTRL00	0x00	RW	Bit[7]: Strobe request ON/OFF Bit[6]: Strobe polarity 0: Active high 1: Active low Bit[5:4]: Pulse width in xenon mode Bit[2:0]: Strobe mode select 000: Xenon 001: LED1 010: LED2 011: LED3 100: LED4
0x3B02	STROBE DMY H	0x00	RW	Dummy Lines Added in Strobe Mode, MSB
0x3B03	STROBE DMY L	0x00	RW	Dummy Lines Added in Strobe Mode, LSB

table 4-7 LED strobe control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B04	STROBE CTRL01	0x00	RW	Bit[3]: start_point_sel Bit[2]: Strobe repeat enable Bit[1:0]: Strobe latency 00: Strobe generated at next frame 01: Strobe generated 2 frames later 10: Strobe generated 3 frames later 11: Strobe generated 4 frames later
0x3B05	STROBE CTRL02	0x00	RW	Bit[7:2]: Strobe pulse width step Bit[1:0]: Strobe pulse width gain Strobe_pulse_width = 128×(2^gain)×(step+1)×Tsclk

4.8 3D application capability

In a 3D camera application, controlling two sensors' rolling shutters with identical timing is important, especially when using an LED or flash during image capture. The OV13850 supports 3D camera applications as shown in the block diagram of **figure 4-11**. A hardware pin (SID) is configured for two different SCCB device addresses. The FSIN pin is used to synchronize the VSYNC signal from the other sensor.

Register 0x3823 = 0x30 to set slave into VSYNC mode. Registers 0x3826 and 0x3827 control slave sensor row reset timing and match master sensor. Registers 0x3824 and 0x3825 control column reset timing. The sensor must have a fixed 0x3824~0x3827 values to match the VSYNC from the other sensor in each video format (size, frame rate, exposure...).

figure 4-11 block diagram of 3D applications

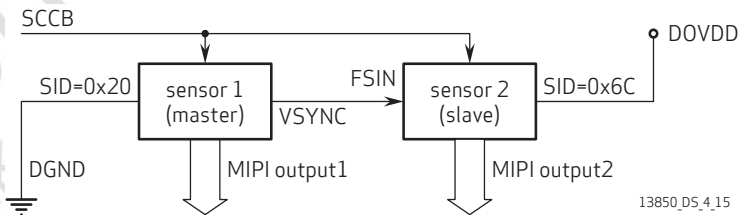


table 4-8 vertical signal synchronize control registers

address	register name	default value	R/W	description
0x3823	REG23	0x00	RW	Bit[7]: fmt_chg_min_dly WO Bit[6]: ext_vs_re Bit[5]: ext_vs_en Bit[4]: r_init_man Bit[3]: vts_no_latch Bit[2:0]: ablc_adj
0x3824	CS_RST_FSIN	0x00	RW	Bit[7:0]: cs reset value at vs_ext[15:8]
0x3825	CS_RST_FSIN	0x00	RW	Bit[7:0]: cs reset value at vs_ext[7:0]
0x3826	R_RST_FSIN	0x00	RW	Bit[7:0]: r reset value at vs_ext[15:8]
0x3827	R_RST_FSIN	0x00	RW	Bit[7:0]: r reset value at vs_ext[7:0]

5 image sensor processor digital functions

5.1 ISP general controls

The ISP module provides several controls including lens correction, and defect pixel cancellation.

table 5-1 ISP general control registers

address	register name	default value	R/W	description
0x5000	R ISP CTRL0	0x08	RW	Bit[3]: Windowing enable Bit[2]: Black defect pixel cancellation enable 0: Disable 1: Enable Bit[1]: White defect pixel cancellation enable 0: Disable 1: Enable Bit[0]: LENC enable
0x5001	R ISP CTRL1	0x01	RW	Bit[3]: Digital gain enable Bit[1]: MWB enable Bit[0]: BLC enable
0x5005	R ISP CTRL5	0x1C	RW	Bit[4]: MWB bias ON This will subtract the BLC target before MWB gain and add the target back after MWB 0: Disable 1: Enable

5.2 LENC

The lens correction (LENC) algorithm compensates for the illumination drop off in the corners due to the lens. Based on the radius of each pixel, the algorithm calculates a gain for each pixel and then corrects each pixel with the calculated gain to compensate for the light distribution due to the lens curvature. Additionally, LENC supports subsampling in both the horizontal and vertical directions. LENC is performed in the RGB domain.

Luminance channel consists of 36 control points while each color channel consists of 25 control points.

figure 5-1 control points of luminance and color channels

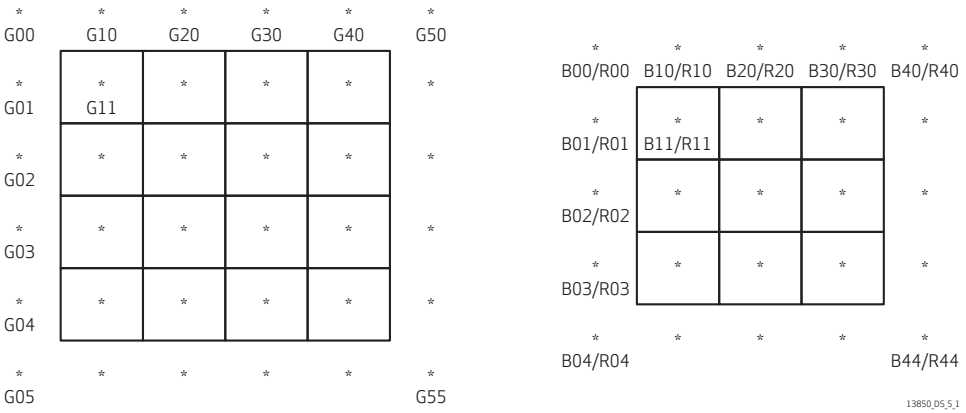


figure 5-2 luminance compensation level calculation

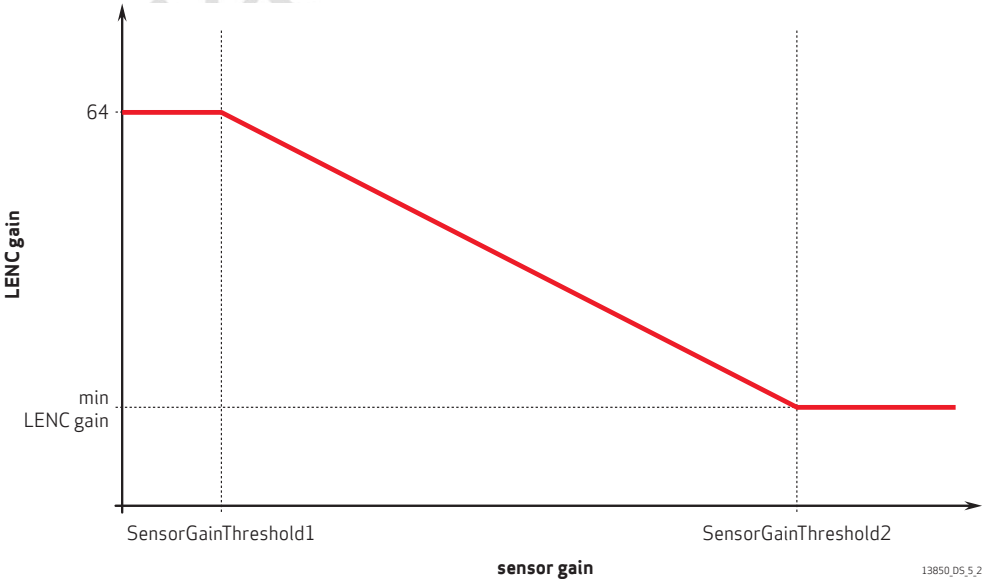


table 5-2 LENC registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5000	R ISP CTRL0	0x08	RW	Bit[0]: LENC enable
0x5200	LENC G00	0x10	RW	Bit[7:0]: Control point G00 for luminance compensation
0x5201	LENC G01	0x10	RW	Bit[7:0]: Control point G01 for luminance compensation
0x5202	LENC G02	0x10	RW	Bit[7:0]: Control point G02 for luminance compensation
0x5203	LENC G03	0x10	RW	Bit[7:0]: Control point G03 for luminance compensation
0x5204	LENC G04	0x10	RW	Bit[7:0]: Control point G04 for luminance compensation
0x5205	LENC G05	0x10	RW	Bit[7:0]: Control point G05 for luminance compensation
0x5206	LENC G10	0x10	RW	Bit[7:0]: Control point G10 for luminance compensation
0x5207	LENC G11	0x08	RW	Bit[7:0]: Control point G11 for luminance compensation
0x5208	LENC G12	0x08	RW	Bit[7:0]: Control point G12 for luminance compensation
0x5209	LENC G13	0x08	RW	Bit[7:0]: Control point G13 for luminance compensation
0x520A	LENC G14	0x08	RW	Bit[7:0]: Control point G14 for luminance compensation
0x520B	LENC G15	0x10	RW	Bit[7:0]: Control point G15 for luminance compensation
0x520C	LENC G20	0x10	RW	Bit[7:0]: Control point G20 for luminance compensation
0x520D	LENC G21	0x08	RW	Bit[7:0]: Control point G21 for luminance compensation
0x520E	LENC G22	0x00	RW	Bit[7:0]: Control point G22 for luminance compensation
0x520F	LENC G23	0x00	RW	Bit[7:0]: Control point G23 for luminance compensation
0x5210	LENC G24	0x08	RW	Bit[7:0]: Control point G24 for luminance compensation
0x5211	LENC G25	0x10	RW	Bit[7:0]: Control point G25 for luminance compensation

note
There is a lens calibration tool that can be used for calibrating these settings required for a specific module. Contact your local OmniVision FAE for generating these settings.

table 5-2 LENC registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5212	LENC G30	0x10	RW	Bit[7:0]: Control point G30 for luminance compensation
0x5213	LENC G31	0x08	RW	Bit[7:0]: Control point G31 for luminance compensation
0x5214	LENC G32	0x00	RW	Bit[7:0]: Control point G32 for luminance compensation
0x5215	LENC G33	0x00	RW	Bit[7:0]: Control point G33 for luminance compensation
0x5216	LENC G34	0x08	RW	Bit[7:0]: Control point G34 for luminance compensation
0x5217	LENC G35	0x10	RW	Bit[7:0]: Control point G35 for luminance compensation
0x5218	LENC G40	0x10	RW	Bit[7:0]: Control point G40 for luminance compensation
0x5219	LENC G41	0x08	RW	Bit[7:0]: Control point G41 for luminance compensation
0x521A	LENC G42	0x08	RW	Bit[7:0]: Control point G42 for luminance compensation
0x521B	LENC G43	0x08	RW	Bit[7:0]: Control point G43 for luminance compensation
0x521C	LENC G44	0x08	RW	Bit[7:0]: Control point G44 for luminance compensation
0x521D	LENC G45	0x10	RW	Bit[7:0]: Control point G45 for luminance compensation
0x521E	LENC G50	0x10	RW	Bit[7:0]: Control point G50 for luminance compensation
0x521F	LENC G51	0x10	RW	Bit[7:0]: Control point G51 for luminance compensation
0x5220	LENC G52	0x10	RW	Bit[7:0]: Control point G52 for luminance compensation
0x5221	LENC G53	0x10	RW	Bit[7:0]: Control point G53 for luminance compensation
0x5222	LENC G54	0x10	RW	Bit[7:0]: Control point G54 for luminance compensation
0x5223	LENC G55	0x10	RW	Bit[7:0]: Control point G55 for luminance compensation

table 5-2 LENC registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x5224	LENC BR00	0xAA	RW	Bit[7:4]: Control point B00 for blue channel compensation Bit[3:0]: Control point R00 for red channel compensation
0x5225	LENC BR01	0xAA	RW	Bit[7:4]: Control point B01 for blue channel compensation Bit[3:0]: Control point R01 for red channel compensation
0x5226	LENC BR02	0xAA	RW	Bit[7:4]: Control point B02 for blue channel compensation Bit[3:0]: Control point R02 for red channel compensation
0x5227	LENC BR03	0xAA	RW	Bit[7:4]: Control point B03 for blue channel compensation Bit[3:0]: Control point R03 for red channel compensation
0x5228	LENC BR04	0xAA	RW	Bit[7:4]: Control point B04 for blue channel compensation Bit[3:0]: Control point R04 for red channel compensation
0x5229	LENC BR10	0xAA	RW	Bit[7:4]: Control point B10 for blue channels compensation Bit[3:0]: Control point R10 for red channels compensation
0x522A	LENC BR11	0x99	RW	Bit[7:4]: Control point B11 for blue channels compensation Bit[3:0]: Control point R11 for red channels compensation
0x522B	LENC BR12	0x99	RW	Bit[7:4]: Control point B12 for blue channels compensation Bit[3:0]: Control point R12 for red channels compensation
0x522C	LENC BR13	0x99	RW	Bit[7:4]: Control point B13 for blue channels compensation Bit[3:0]: Control point R13 for red channels compensation
0x522D	LENC BR14	0xAA	RW	Bit[7:4]: Control point B14 for blue channels compensation Bit[3:0]: Control point R14 for red channels compensation

table 5-2 LENC registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x522E	LENC BR20	0xAA	RW	Bit[7:4]: Control point B20 for blue channels compensation Bit[3:0]: Control point R20 for red channels compensation
0x522F	LENC BR21	0x99	RW	Bit[7:4]: Control point B21 for blue channels compensation Bit[3:0]: Control point R21 for red channels compensation
0x5230	LENC BR22	0x88	RW	Bit[7:4]: Control point B22 for blue channels compensation Bit[3:0]: Control point R22 for red channels compensation
0x5231	LENC BR23	0x99	RW	Bit[7:4]: Control point B23 for blue channels compensation Bit[3:0]: Control point R23 for red channels compensation
0x5232	LENC BR24	0xAA	RW	Bit[7:4]: Control point B24 for blue channels compensation Bit[3:0]: Control point R24 for red channels compensation
0x5233	LENC BR30	0xAA	RW	Bit[7:4]: Control point B30 for blue channels compensation Bit[3:0]: Control point R30 for red channels compensation
0x5234	LENC BR31	0x99	RW	Bit[7:4]: Control point B31 for blue channels compensation Bit[3:0]: Control point R31 for red channels compensation
0x5235	LENC BR32	0x99	RW	Bit[7:4]: Control point B32 for blue channels compensation Bit[3:0]: Control point R32 for red channels compensation
0x5236	LENC BR33	0x99	RW	Bit[7:4]: Control point B33 for blue channels compensation Bit[3:0]: Control point R33 for red channels compensation
0x5237	LENC BR34	0xAA	RW	Bit[7:4]: Control point B34for blue channels compensation Bit[3:0]: Control point R34 for red channels compensation

table 5-2 LENC registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5238	LENC BR40	0xAA	RW	Bit[7:4]: Control point B40 for blue channels compensation Bit[3:0]: Control point R40 for red channels compensation
0x5239	LENC BR41	0xAA	RW	Bit[7:4]: Control point B41 for blue channels compensation Bit[3:0]: Control point R41 for red channels compensation
0x523A	LENC BR42	0xAA	RW	Bit[7:4]: Control point B42 for blue channels compensation Bit[3:0]: Control point R4 for red channels compensation
0x523B	LENC BR43	0xAA	RW	Bit[7:4]: Control point B43 for blue channels compensation Bit[3:0]: Control point R43 for red channels compensation
0x523C	LENC BR44	0xAA	RW	Bit[7:4]: Control point B44 for blue channels compensation Bit[3:0]: Control point R44 for red channels compensation
0x523D	LENC BR OFFSET	0x88	RW	Bit[7:4]: Base value for all blue channel control points Bit[3:0]: Base value for all red channel control points
0x523E	MAXGAIN	0x40	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will be the minimum value (min LENC gain). Register value is 16 times sensor gain.
0x523F	MINGAIN	0x20	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will start to decrease; otherwise, the amplitude will not change. Register value is 16 times sensor gain.

table 5-2 LENC registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x5240	MINQ	0x18	RW	Bit[6:0]: This value indicates the minimum amplitude which luminance channel compensates when AutoLensSwitchEnable is true. Value should be in the range [0~64]

5.3 defect pixel cancellation (DPC)

Primarily due to process anomalies, pixel defects in the sensor array will occur, generating incorrect pixel levels and color values. The purpose of the DPC is to remove the effects caused by defective pixels.

table 5-3 DPC control registers

address	register name	default value	R/W	description
0x5000	R ISP CTRL0	0x08	RW	Bit[2]: Remove black defect pixel 0: Disable 1: Enable Bit[1]: Remove white defect pixel 0: Disable 1: Enable

5.4 white balance, exposure and gain control

5.4.1 manual white balance (MWB)

The MWB provides digital gain for R, G, and B channels. Each channel gain is 12-bit. 0x400 is 1x gain.

table 5-4 MWB control registers

address	register name	default value	R/W	description
0x5056	RED GAIN	0x04	RW	Bit[3:0]: MWB red gain[11:8] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x5057	RED GAIN	0x00	RW	Bit[7:0]: MWB red gain[7:0] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x5058	GRN GAIN	0x04	RW	Bit[3:0]: MWB green gain[11:8] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x5059	GRN GAIN	0x00	RW	Bit[3:0]: MWB green gain[7:0] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x505A	BLU GAIN	0x04	RW	Bit[3:0]: MWB blue gain[11:8] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400
0x505B	BLU GAIN	0x00	RW	Bit[7:0]: MWB blue gain[7:0] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400
0x5001	R ISP CTRL1	0x01	RW	Bit[1]: MWB gain enable 0: Disable 1: Enable

5.4.2 manual exposure control (MEC)

Manual exposure provides exposure time settings. The exposure value in register 0x3500~0x3502 is in units of 1/16 line.

table 5-5 MEC control registers

address	register name	default value	R/W	description
0x3500	AEC LONG EXPO	0x00	RW	Long Exposure Bit[3:0]: Long exposure[19:16]
0x3501	AEC LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[15:8]
0x3502	AEC LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0.
0x3503	AEC MANUAL	0x03	RW	AEC Manual Mode Control Bit[5]: Gain delay option 0: 1 frame latch 1: Delay 1 frame latch Bit[4]: Choose delay option 0: Delay disable 1: Delay enable Bit[2]: VTS manual enable There is no auto module in this device so this bit should always be 1 1: Manual enable Bit[1]: AGC manual enable There is no auto module in this device so this bit should always be 1 1: Manual enable Bit[0]: AEC manual enable There is no auto module in this device so this bit should be always 1 1: Manual enable
0x3506	AEC SHORT EXPO	0x00	RW	Short Exposure Bit[3:0]: Short exposure[19:16]
0x3507	AEC SHORT EXPO	0x02	RW	Short Exposure Bit[7:0]: Short exposure[15:8]
0x3508	AEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0.

5.4.3 manual gain control (MGC)

Manual gain provides analog gain settings. The OV13850 has a maximum 16x analog gain.

table 5-6 MGC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3504	MAN SNR GAIN LONG	0x00	RW	Manual Sensor Long Gain Bit[1:0]: Manual sensor gain[9:8]
0x3505	MAN SNR GAIN LONG	0x00	RW	Manual Sensor Long Gain Bit[7:0]: Manual sensor gain[7:0]
0x3509	AEC GAIN CONVERT	0x10	RW	AEC Manual Mode Control Bit[4]: Long sensor gain convert enable 0: Use sensor gain {0x350A,0x350B} as sensor gain 1: Use real gain {0x350A,0x350B} as real gain Bit[3]: Long sensor gain manual enable 0: Disable 1: Manual control {0x3504,0x3505}, cannot trigger BLC with these gain registers Bit[1]: Short sensor gain convert enable 0: Use sensor gain {0x350E,0x350F} as sensor gain long 1: Use real gain {0x350E,0x350F} as real gain Bit[0]: Short sensor gain manual enable 0: Disable 1: Manual control {0x3514,0x3515}, cannot trigger BLC with these gain registers
0x350A	GAIN LONG PK	0x00	RW	Long Gain Output to Sensor Bit[2:0]: Gain[10:8]

table 5-6 MGC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x350B	GAIN LONG PK	0x10	RW	Long Gain Output to Sensor Bit[7:0]: Gain[7:0] When 0x3509[4] = 0, this gain is sensor gain. Real gain = 2^n(16+x)/16 where N is number of 1 in bits gain[9:4] and X is the low bits gain[3:0] When 0x3509[4] = 1, this gain is real gain. Low 4 bits are fraction bits.
0x350E	GAIN SHORT PK	0x00	RW	Short Gain Output to Sensor Bit[2:0]: Gain[10:8]
0x350F	GAIN SHORT PK	0x10	RW	Short Gain Output to Sensor Bit[7:0]: Gain[7:0] When 0x3509[4] = 0, this gain is sensor gain. Real gain = 2^n(16+x)/16 where N is number of 1 in bits gain[9:4] and X is the low bits gain[3:0] When 0x3509[4] = 1, this gain is real gain. Low 4 bits are fraction bits.
0x3514	MAN SNR GAIN SHORT	0x00	RW	Manual Sensor Short Gain Bit[1:0]: Manual sensor gain[9:8]
0x3515	MAN SNR GAIN SHORT	0x00	RW	Manual Sensor Short Gain Bit[7:0]: Manual sensor gain[7:0]

6 register tables

The following tables provide descriptions of the device control registers contained in the OV13850. The device slave addresses are 0x20 for write and 0x21 for read when SID= 0, 0x6C for write and 0x6D for read when SID= 1.

6.1 system control [0x0100 - 0x303E]

table 6-1 system control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x0100	MODE_SELECT	0x00	RW	Bit[7:1]: Not used Bit[0]: Mode select 0: software_standby 1: Streaming
0x0102	FAST_STANDBY	0x00	RW	Bit[7:1]: Not used Bit[0]: Fast standby 0: Vblanking standby 1: Immediate standby
0x0103	SOFTWARE_RST	–	W	Bit[7:1]: Not used Bit[0]: software_reset
0x3002	SC_PAD_OEN0	0x80	RW	Bit[7]: io_vsync_oen Bit[6]: io_href_oen Bit[5]: Debug mode Bit[4]: io_frex_oen Bit[3]: io_fsin_oen Bit[2]: Debug mode Bit[1]: io_gpio1_oen Bit[0]: io_gpio0_oen
0x3005	SC_PAD_OUT2	0x00	RW	Bit[7]: io_vsync_o Bit[6]: io_href_o Bit[5]: io_il_pwm Bit[4]: io_frex_o Bit[3]: io_fsin_o Bit[2]: io_strobe_o Bit[1]: io_gpio1_o Bit[0]: io_gpio0_o
0x3008	PAD_SEL2	0x00	RW	Bit[7]: io_vsync_sel Bit[6]: io_href_sel Bit[5]: io_frex_sel Bit[4]: io_strobe_sel Bit[3]: io_fsin_sel Bit[2]: io_il_pwm_sel Bit[1]: io_gpio1_sel Bit[0]: io_gpio0_sel

table 6-1 system control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x3009	PAD_CTRL	0x06	RW	Bit[7]: Debug mode Bit[6:5]: iP2X3v Bit[4:3]: Debug mode Bit[2]: pad_fsin_enb Bit[1]: pad_frex_enb Bit[0]: Debug mode
0x300A	SC_CHIP_ID	0xD8	R	Chip ID High Byte
0x300B	SC_CHIP_ID	0x50	R	Chip ID Low Byte
0x300C	SC_SCCB_ID	0x20	RW	SCCB ID
0x300D	PUMP_CLK_CTRL	0x15	RW	Bit[7]: Debug mode Bit[6:4]: p_pump_clk_div Bit[2:0]: n_pump_clk_div
0x300E	PLL_CTRL1	0x00	RW	Bit[7:5]: Debug mode Bit[4]: scale_div_man_en Bit[3:0]: pll_scale_div
0x300F	MIPI_SC	0x11	RW	Bit[7:5]: Debug mode Bit[4]: mipi_en Bit[3:2]: Debug mode Bit[1:0]: mipi_bit 00: 8-bit mode 01: 10-bit mode 10: 12-bit mode 11: Reserved
0x3010	MIPI_PHY[15:8]	0x00	RW	Bit[7:5]: slew_rate[2:0] Bit[4]: pgm_bp_hs_en_lat Bypass latch of hs_enable Bit[3]: Relatch Bit[2:0]: pgm_vcm[1:0] High speed common mode voltage
0x3011	MIPI_PHY[7:0]	0x74	RW	Bit[7:4]: sel_drv Bit[3:2]: pgm_lptx Bit[1:0]: r_iref

table 6-1 system control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x3012	MIPI_SC_CTRL0	0x41	RW	Bit[7:4]: lane_num 0000: 0 lane 0001: 1 lane 0010: 2 lanes 0100: 4 lanes Bit[3]: mipi_phy_rst_o Bit[2]: r_phy_pd_mipi 1: Power down PHY HS TX Bit[1]: r_phy_pd_lprx 1: Power down PHY LP RX module Bit[0]: phy_pad_en
0x3013	MIPI_SC_CTRL1	0x00	RW	Bit[7]: Debug mode Bit[6:4]: mipi_d2_skew Bit[3]: Debug mode Bit[2:0]: mipi_d1_skew
0x3014	MIPI_SC_CTRL2	0x00	RW	Bit[7]: Debug mode Bit[6:4]: mipi_d4_skew Bit[3]: Debug mode Bit[2:0]: mipi_d3_skew
0x3015	MIPI_SC_CTRL3	0x00	RW	Bit[7]: mipi_lane_dis4 Bit[6]: mipi_lane_dis3 Bit[5]: mipi_lane_dis2 Bit[4]: mipi_lane_dis1 Bit[3]: mipi_ck_lane_dis Bit[2]: mipi_lp_sr Bit[1:0]: mipi_ck_skew_o
0x3016	SC_CLKRST0	0xF0	RW	Bit[7]: sclk_ac Bit[6]: sclk_stb Bit[5]: sclk_ofc Bit[4]: sclk_tc Bit[3]: rst_ac Bit[2]: rst_stb Bit[1]: rst_ofc Bit[0]: rst_tc
0x3017	SC_CLKRST1	0xF0	RW	Bit[7]: sclk_tpm Bit[6]: sclk_isp Bit[5]: sclk_arb Bit[4]: sclk_vfifo Bit[3]: rst_tpm Bit[2]: rst_isp Bit[1]: rst_arb Bit[0]: rst_vfifo

table 6-1 system control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x3018	SC_CLKRST2	0xF0	RW	Bit[7]: Debug mode Bit[6]: sclk_mipi Bit[5]: sclk_hsub Bit[4]: sclk_otp Bit[3]: Debug mode Bit[2]: rst_mipi Bit[1]: rst_hsub Bit[0]: rst_otp
0x3019	SC_CLKRST3	0xF0	RW	Bit[7]: sclk_blc Bit[6]: sclk_ispfc Bit[5]: sclk_fmt Bit[4]: sclk_embline Bit[3]: rst_blc Bit[2]: rst_ispfc Bit[1]: rst_fmt Bit[0]: rst_embline
0x301A	SC_CLKRST4	0xF0	RW	Bit[7]: sclk_grp Bit[6]: padclk_mipi_sc Bit[5]: pclk_vfifo Bit[4]: pclk_mipi Bit[3]: rst_grp Bit[2]: rst_mipi_sc Bit[1]: rst_illum Bit[0]: Debug mode
0x301B	SC_CLKRST5	0xB4	RW	Bit[7:6]: dac_clk_sel Bit[5]: sclk_bist20 Bit[4]: sclk_snr_sync Bit[3]: sclk_grp_fix Bit[2]: dacclk_en Bit[1]: rst_bist20 Bit[0]: rst_snr_sync
0x301C	SC_FREX_RST_MASK0	0x01	RW	Bit[7]: Debug mode Bit[6]: frex_mask_illum_disable Bit[5]: frex_mask_sync_fifo_disable Bit[4]: frex_mask_emb_disable Bit[3]: frex_mask_ispfc_disable Bit[2]: frex_mask_blc_fmt_disable Bit[1]: frex_mask_fc_disable Bit[0]: frex_mask_stb_disable
0x301D	SC_FREX_RST_MASK1	0x02	RW	Bit[7]: frex_mask_ofc_disable Bit[6]: frex_mask_tpm_disable Bit[5]: frex_mask_isp_disable Bit[4]: frex_mask_dvp_disable Bit[3]: frex_mask_mipi_disable Bit[2]: frex_mask_vfifo_fmt_disable Bit[1]: frex_mask_arb_disable Bit[0]: frex_mask_mipi_phy_disable

table 6-1 system control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x301E	SC_CLOCK_SEL	0x00	RW	Bit[7:5]: sdiv Divider for sigma-delta 0: Use pll_pclk_i for sclk 1: Use pll_sclk_i for sclk Bit[4]: Debug mode Bit[3]: pclk_sel Bit[2:1]: sclk_sel Bit[0]: sclk2x_sel
0x301F	SC_MISC_CTRL	0x03	RW	Bit[7:1]: Debug mode Bit[0]: cen_global_o
0x3020	LOW_PWR_CTR	0x00	RW	Bit[7]: Debug mode Bit[6]: phy_pd_mipi_pwdn_dis Bit[5]: phy_pd_lprx_pwdn_dis Bit[4]: stb_rst_dis 0: Reset all blocks at software standby mode 1: TC, sensor_control, ISP are reset, others not Bit[3]: pd_ana_dis Bit[2]: pd_big_regulator_dis Bit[1]: phy_pd_mipi_slppd_dis Bit[0]: phy_pd_lprx_slppd_dis
0x302A	SC_CHIP_REVISION	0xB0	R	Chip Revision
0x303D	SC_GP_IO_IN0	–	R	Bit[7:5]: Debug mode Bit[4]: tpm_db Bit[3:0]: Debug mode
0x303E	SC_GP_IO_IN1	–	R	Bit[7]: Debug mode Bit[6:5]: p_gpio_i Bit[4]: p_vsync_i Bit[3]: p_href_i Bit[2:0]: Debug mode

6.2 PLL1 [0x0300 - 0x030A]

table 6-2 PLL1 registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x0300	PLL1_CTRL_0	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: PLL1_PREDIV 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0301	PLL1_CTRL_1	0x00	RW	Bit[7:23]: Debug mode Bit[1:0]: PLL1_DIVP[9:8]
0x0302	PLL1_CTRL_2	0x2A	RW	Bit[7:0]: PLL1_DIVP[7:0]
0x0303	PLL1_CTRL_3	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: PLL1_DIVM 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16
0x0304	PLL1_CTRL_4	0x03	RW	Bit[7:2]: Debug mode Bit[1:0]: PLL1_DIV_MIPI 00: /4 01: /5 10: /6 11: /8

table 6-2 PLL1 registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x0305	PLL1_CTRL_5	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: PLL1_DIV_SP 00: /3 01: /4 10: /5 11: /6
0x0306	PLL1_CTRL_6	0x01	RW	Bit[7:1]: Debug mode Bit[0]: PLL1_DIV_S 0: /1 1: /2
0x0308	PLL1_CTRL_8	0x00	RW	Bit[7:1]: Debug mode Bit[0]: PLL1_bypass
0x0309	PLL1_CTRL_9	0x01	RW	Bit[7:31]: Debug mode Bit[2:0]: PLL1_CP
0x030A	PLL1_CTRL_A	0x00	RW	Bit[7:1]: Debug mode Bit[0]: PLL1_PREDIVP 0: /1 1: /2

6.3 PLL2 control [0x3600 - 0x3615]

table 6-3 PLL2 registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3600~ 0x360F	ANALOG CTRL	–	–	Analog Control Registers
0x3610	ASP_CTRL16	0x00	RW	Bit[7:5]: R_TPM[7:5] Empty Bit[4:0]: R_TPM[4:0] Temperature meter trimming

table 6-3 PLL2 registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3611	ASP_CTRL17	0x10	RW	Bit[7]: PLL2_bypass 0: Working 1: Bypass Bit[6:4]: PLL2_CP Default 001 Bit[3]: PLL2_PREDIVP 0: By 1 1: By 2 Bit[2:0]: PLL2_PREDIV 000: 1 001: 1.5 010: 2 011: 2.5 100: 3 101: 4 110: 6 111: 8
0x3612	ASP_CTRL18	0x23	RW	Bit[7]: Power down pump clock divider 0: Working 1: Power down Bit[6:4]: PLL2_DIVS System clock divider control bits 000: 1 001: 1.5 010: 2 011: 2.5 100: 3 101: 3.5 110: 4 111: 5 Bit[3:0]: PLL2_DIVSP System clock pre_divider control bit value = [3:0] + 1
0x3613	ASP_CTRL19	0x33	RW	Bit[7:4]: PLL2_DIVSRAM SRAM clock divider control bit value = [3:0] + 1 Bit[3:0]: PLL2_DIVDAC DAC clock divider control bit value = [3:0] + 1
0x3614	ASP_CTRL20	0x28	RW	Bit[7:0]: PLL2_DIVP[7:0] Loop divider control value = [9:0]

table 6-3 PLL2 registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3615	ASP_CTRL21	0x1C	RW	Bit[7:6]: Debug mode Bit[5:4]: N_pump clock div[1:0] Div number 00: /2 01: /3 10: /4 11: /8 Bit[3:2]: P_pump clock div[1:0] Div number 00: /2 01: /3 10: /4 11: /8 Bit[1:0]: PLL2_DIVP[9:8]

6.4 SCCB [0x3100 - 0x3104]

table 6-4 SCCB control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3100	SB_SCCB_CTRL	0x00	RW	Bit[7:4]: Debug mode Bit[3]: r_sda_dly_en Bit[2:0]: r_sda_dly
0x3101	SB_SCCB_OPT	0x12	RW	Bit[7:5]: Debug mode Bit[4]: en_ss_addr_inc Bit[3]: r_sda_byp_sync 0: Two clock stage sync for sda_i 1: No sync for sda_i Bit[2]: r_scl_byp_sync 0: Two clock stage sync for scl_i 1: No sync for scl_i Bit[1]: r_msk_glitch Bit[0]: r_msk_stop
0x3102	SB_SCCB_FILTER	0x00	RW	Bit[7:4]: r_sda_num Bit[3:0]: r_scl_num
0x3103	DEBUG MODE	–	–	Debug Mode

table 6-4 SCCB control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3104	PLL_BYP_RST	0x00	RW	Bit[7:5]: Debug mode Bit[4]: srb_clk_sync_en Bit[3:2]: wkup_wait_time_opt Bit[1]: pll_clk_sel Bit[0]: Reserved

6.5 group hold [0x3200 - 0x3213]

table 6-5 group hold registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM, Actual Address is {0x3200[3:0], 0x0}
0x3201	GROUP ADR1	0x08	RW	Group1 Start Address in SRAM, Actual Address is {0x3201[3:0], 0x0}
0x3202	GROUP ADR2	0x10	RW	Group2 Start Address in SRAM, Actual Address is {0x3202[3:0], 0x0}
0x3203	GROUP ADR3	0x18	RW	Group3 Start Address in SRAM, Actual Address is {0x3203[3:0], 0x0}
0x3204	GROUP LEN0	–	W	Length of Group0
0x3205	GROUP LEN1	–	W	Length of Group1
0x3206	GROUP LEN2	–	W	Length of Group2
0x3207	GROUP LEN3	–	W	Length of Group3
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch Others: Debug mode Bit[3:0]: group ID 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3 Others: Debug mode
0x3209	GROUP0 PERIOD	0x00	RW	Number of Frames to Stay in Group 0
0x320A	GROUP1 PERIOD	0x00	RW	Number of Frames to Stay in Group 1

table 6-5 group hold registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x320B	GRP_SW_CTRL	0x01	RW	Bit[7]: auto_sw Bit[6:5]: Debug mode Bit[4]: frame_cnt_trig Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: Second group select
0x320C	DEBUG MODE	–	–	Debug Mode
0x320D	GRP_ACT	–	R	Active Group Indicator
0x320E	FM_CNT_GRP0	–	R	Group 0 Frame Count
0x320F	FM_CNT_GRP1	–	R	Group 1 Frame Count
0x3210~ 0x3213	DEBUG MODE	–	–	Debug Mode

6.6 strobe [0x3B00 - 0x3B05]

table 6-6 strobe control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE CTRL0	0x00	RW	Bit[7]: STROBE on/off Bit[6]: STROBE polarity 0: Active high 1: Active low Bit[5:4]: width_in_xenon Bit[2:0]: Mode 000: Xenon 001: LED1 010: LED2 011: LED3 100: LED4
0x3B02	STROBE DMY H	0x00	RW	Dummy Lines Added At Strobe Mode, MSB
0x3B03	STROBE DMY L	0x00	RW	Dummy Lines Added At Strobe Mode, LSB
0x3B04	STROBE CTRL1	0x00	RW	Bit[7:4]: Debug mode Bit[3]: Start_point_sel Bit[2]: Strobe repeat enable Bit[1:0]: Strobe latency 00: Strobe generated at next frame 01: Strobe generated 2 frames later 10: Strobe generated 3 frames later 11: Strobe generated 4 frames later

table 6-6 strobe control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B05	STROBE WIDTH	0x00	RW	Bit[7:2]: Strobe pulse width step Bit[1:0]: Strobe pulse width gain strobe_pulse_width = 128 x (2^gain) x (step+1) x Tsclk

6.7 MEC control [0x3500 - 0x3508]

table 6-7 MEC control registers

address	register name	default value	R/W	description
0x3500	AEC LONG EXPO	0x00	RW	Long Exposure Bit[3:0]: Long exposure[19:16]
0x3501	AEC LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[15:8]
0x3502	AEC LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0.
0x3503	AEC MANUAL	0x03	RW	AEC Manual Mode Control Bit[5]: Gain delay option 0: 1 frame latch 1: Delay 1 frame latch Bit[4]: Choose delay option 0: Delay disable 1: Delay enable Bit[2]: VTS manual enable There is no auto module in this device so this bit should always be 1 1: Manual enable Bit[1]: AGC manual enable There is no auto module in this device so this bit should always be 1 1: Manual enable Bit[0]: AEC manual enable There is no auto module in this device so this bit should be always 1 1: Manual enable
0x3506	AEC SHORT EXPO	0x00	RW	Short Exposure Bit[3:0]: Short exposure[19:16]
0x3507	AEC SHORT EXPO	0x02	RW	Short Exposure Bit[7:0]: Short exposure[15:8]
0x3508	AEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0.

6.8 MGC control [0x3504 - 0x3515]

table 6-8 MGC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3504	MAN SNR GAIN LONG	0x00	RW	Manual Sensor Long Gain Bit[7:2]: Debug mode Bit[1:0]: Manual sensor gain[9:8]
0x3505	MAN SNR GAIN LONG	0x00	RW	Manual Sensor Long Gain Bit[7:0]: Manual sensor gain[7:0]
0x3509	AEC GAIN CONVERT	0x10	RW	AEC Manual Mode Control Bit[7:5]: Debug mode Bit[4]: Long sensor gain convert enable 0: Use sensor gain {0x350A,0x350B} as sensor gain 1: Use real gain {0x350A,0x350B} as real gain Bit[3]: Long sensor gain manual enable 0: Disable 1: Manual control {0x3504,0x3505}, cannot trigger BLC with these gain registers Bit[1]: Short sensor gain convert enable 0: Use sensor gain {0x350E,0x350F} as sensor gain long 1: Use real gain {0x350E,0x350F} as real gain Bit[0]: Short sensor gain manual enable 0: Disable 1: Manual control {0x3514,0x3515}, cannot trigger BLC with these gain registers
0x350A	GAIN LONG PK	0x00	RW	Long Gain Output to Sensor Bit[7:3]: Debug mode Bit[2:0]: Gain[10:8]

table 6-8 MGC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x350B	GAIN LONG PK	0x10	RW	Long Gain Output to Sensor Bit[7:0]: Gain[7:0] When 0x3509[4] = 0, this gain is sensor gain. Real gain = 2^n(16+x)/16 where N is number of 1 in bits gain[9:4] and X is the low bits gain[3:0] When 0x3509[4] = 1, this gain is real gain. Low 4 bits are fraction bits.
0x350E	GAIN SHORT PK	0x00	RW	Short Gain Output to Sensor Bit[7:3]: Debug mode Bit[2:0]: Gain[10:8]
0x350F	GAIN SHORT PK	0x10	RW	Short Gain Output to Sensor Bit[7:0]: Gain[7:0] When 0x3509[4] = 0, this gain is sensor gain. Real gain = 2^n(16+x)/16 where N is number of 1 in bits gain[9:4] and X is the low bits gain[3:0] When 0x3509[4] = 1, this gain is real gain. Low 4 bits are fraction bits.
0x3514	MAN SNR GAIN SHORT	0x00	RW	Manual Sensor Short Gain Bit[7:2]: Debug mode Bit[1:0]: Manual sensor gain[9:8]
0x3515	MAN SNR GAIN SHORT	0x00	RW	Manual Sensor Short Gain Bit[7:0]: Manual sensor gain[7:0]

6.9 timing control [0x3800 - 0x3835]

table 6-9 timing control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3800	H_CROP_START	0x00	RW	Bit[7:5]: Debug mode Bit[4:0]: Horizontal crop start address[12:8]
0x3801	H_CROP_START	0x20	RW	Bit[7:0]: Horizontal crop start address[7:0]
0x3802	V_CROP_START	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Vertical crop start address[11:8]

table 6-9 timing control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3803	V_CROP_START	0x0C	RW	Bit[7:0]: Vertical crop start address[7:0]
0x3804	H_CROP_END	0x10	RW	Bit[7:5]: Debug mode Bit[4:0]: Horizontal crop end address[12:8]
0x3805	H_CROP_END	0x8B	RW	Bit[7:0]: Horizontal crop end address[7:0]
0x3806	V_CROP_END	0x0C	RW	Bit[7:4]: Debug mode Bit[3:0]: Vertical crop end address[11:8]
0x3807	V_CROP_END	0x43	RW	Bit[7:0]: Vertical crop end address[7:0]
0x3808	H_OURPUT_SIZE	0x10	RW	Bit[7:5]: Debug mode Bit[4:0]: Horizontal output size[12:8]
0x3809	H_OUTPUT_SIZE	0x70	RW	Bit[7:0]: Horizontal output size[7:0]
0x380A	V_OURPUT_SIZE	0x0C	RW	Bit[7:4]: Debug mode Bit[3:0]: Vertical output size[11:8]
0x380B	V_OUTPUT_SIZE	0x30	RW	Bit[7:0]: Vertical output size[7:0]
0x380C	TIMING_HTS	0x12	RW	Bit[7]: Debug mode Bit[6:0]: Horizontal total size[14:8]
0x380D	TIMING_HTS	0xC0	RW	Bit[7:0]: Horizontal total size[7:0]
0x380E	TIMING_VTS	0x0D	RW	Bit[7]: Debug mode Bit[6:0]: Vertical total size[14:8]
0x380F	TIMING_VTS	0x00	RW	Bit[7:0]: Vertical total size[7:0]
0x3810	H_WIN_OFF	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Horizontal windowing offset[11:8]
0x3811	H_WIN_OFF	0x04	RW	Bit[7:0]: Horizontal windowing offset[7:0]
0x3812	V_WIN_OFF	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Vertical windowing offset[11:8]
0x3813	V_WIN_OFF	0x04	RW	Bit[7:0]: Vertical windowing offset[7:0]
0x3814	H_INC	0x11	RW	Bit[7:4]: Horizontal sub-sample odd increase number Bit[3:0]: Horizontal sub-sample even increase number
0x3815	V_INC	0x11	RW	Bit[7:4]: Vertical sub-sample odd increase number Bit[3:0]: Vertical sub-sample even increase number
0x3820	FORMAT 0	0x00	RW	Bit[7:3]: Debug mode Bit[2]: vflip Bit[1]: vbinf Bit[0]: vbin

table 6-9 timing control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3821	FORMAT 1	0x00	RW	Bit[7:3]: Debug mode Bit[2]: Mirror Bit[1]: dig_subsample Bit[0]: hbin
0x382A~ 0x382E	DEBUG MODE	–	–	Debug Mode
0x382F	REG2F	0x04	RW	Bit[7:5]: Debug mode Bit[4]: vsync_polarity Bit[3:0]: vsync_width
0x3830	REG30	0x00	RW	Bit[7:0]: vsync_rising_rcnt[15:8]
0x3831	REG31	0x00	RW	Bit[7:0]: vsync_rising_rcnt[7:0]
0x3832	REG32	0x00	RW	Bit[7:0]: vsync_rising_ccnt[15:8]
0x3833	REG33	0x01	RW	Bit[7:0]: vsync_rising_ccnt[7:0]
0x3834	REG34	0x00	RW	Bit[7:4]: Debug mode Bit[3]: drop_rgb Bit[2]: drop_w Bit[1]: hsub_post Bit[0]: hbin_post
0x3835	REG35	0x14	RW	Bit[4]: cut_en Bit[3]: vts_auto_en Bit[2]: blk_col_dis Bit[1:0]: href_w

6.10 BLC [0x4000 - 0x4041]

table 6-10 BLC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0xF1	RW	Bit[7]: outrange_trig_en Offset out of range trigger function enable signal 0: Disable 1: Enable Bit[6]: format_chg_en Format change trigger function enable signal 0: Disable 1: Enable Bit[5]: gain_chg_en Gain change trigger function enable signal 0: Disable 1: Enable Bit[4]: Not used Bit[3]: manual_trig Manual trigger signal Its rising edge will trigger BLC Bit[2]: freeze_en BLC freeze function enable signal When it is set, the BLC will be frozen. Offsets will keep the their pre-frame values. Bit[1]: always_do BLC always trigger signal When it is set, the BLC will be triggered every frame unless the freeze_en is enabled. Bit[0]: median_en 5-point median filter function enable signal 0: Disable 1: Enable
0x4001	BLC CTRL01	0x00	RW	Bit[7:2]: Not used Bit[1]: blc_cut_range_en Bit[0]: remove_row_offset_en Column delta offset remove function enable signal 0: Used offset does not include column delta offset 1: Used offset includes column delta offset
0x4002	BLC CTRL 02	0x04	RW	Bit[7:0]: offset_lim_value

table 6-10 BLC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4003	BLC CTRL 03	0x14	RW	Bit[7:0: blk_num
0x4004	TARGET	0x00	RW	Bit[7:0]: Target[15:8] Target high 8 bits
0x4005	TARGET	0x10	RW	Bit[7:0]: Target[7:0] Target low 8 bits
0x4006	BLC CTRL 06	0x1F	RW	Bit[7:0]: format_trig_framenumber
0x4007	BLC CTRL 07	0x1F	RW	Bit[7:0]: reset_trig_framenumber
0x4008	BLC CTRL 08	0x01	RW	Bit[7:0]: manual_trig_framenumber
0x4009~ 0x400B	DEBUG MODE	–	–	Debug Mode
0x400C	OFFSET TRIG THRESH	0x00	RW	Bit[7:0]: offset_trig_thresh[15:8]
0x400D	OFFSET TRIG THRESH	0x20	RW	Bit[7:0]: offset_trig_thresh[7:0]
0x400E~ 0x4041	DEBUG MODE	–	–	Debug Mode

6.11 ISP_top [0x5000 - 0x5065]

table 6-11 ISP_top registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	R ISP CTRL0	0x08	RW	Bit[7:4]: Debug mode Bit[3]: Windowing enable Bit[2]: Black defect pixel cancellation enable 0: Disable 1: Enable Bit[1]: White defect pixel cancellation enable 0: Disable 1: Enable Bit[0]: LENC enable

table 6-11 ISP_top registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5001	R ISP CTRL1	0x01	RW	Bit[7:4]: Debug mode Bit[3]: Digital gain enable Bit[2]: Debug mode Bit[1]: MWB enable Bit[0]: BLC enable
0x5002~ 0x5004	DEBUG MODE	–	–	Debug Mode
0x5005	R ISP CTRL5	0x1C	RW	Bit[4]: MWB bias ON This will subtract the BLC target before MWB gain and add the target back after MWB 0: Disable 1: Enable
0x5006~ 0x5055	DEBUG MODE	–	–	Debug Mode
0x5056	RED GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: MWB red gain[11:8] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x5057	RED GAIN	0x00	RW	Bit[7:0]: MWB red gain[7:0] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x5058	GRN GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: MWB green gain[11:8] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x5059	GRN GAIN	0x00	RW	Bit[7:0]: MWB green gain[7:0] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x505A	BLU GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: MWB blue gain[11:8] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400
0x505B	BLU GAIN	0x00	RW	Bit[7:0]: MWB blue gain[7:0] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400

table 6-11 ISP_top registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x505C~ 0x505F	DEBUG MODE	–	–	Debug Mode
0x5060	BIST CTRL1	0x09	RW	Bit[7:4]: Not used Bit[3]: awb_done_vsync Bit[2:0]: awb_done_mask
0x5061~ 0x5065	DEBUG MODE	–	–	Debug Mode

6.12 digital gain [0x5500 - 0x550B]

table 6-12 digital gain registers

address	register name	default value	R/W	description
0x5500	DIGG CTRL00	0x03	RW	Bit[7:5]: Not used Bit[4]: lsb_replace_en Replace the LSB of final output data with the LSB of input data Bit[3:2]: Debug mode Bit[1]: BLC bias switch Bit[0]: Manual digital gain mode
0x5502	DIG GAIN L MAN	0x01	RW	Bit[7:3]: Not used Bit[2:0]: dig_gain_l_man[10:8]
0x5503	DIG GAIN L MAN	0x00	RW	Bit[7:0]: dig_gain_l_man[7:0]
0x5504	DIG GAIN S MAN	0x01	RW	Bit[7:3]: Not used Bit[2:0]: dig_gain_s_man[10:8]
0x5505	DIG GAIN S MAN	0x00	RW	Bit[7:0]: dig_gain_s_man[7:0]
0x5508~ 0x550B	DEBUG MODE	–	–	Debug Mode

6.13 illumination PWM [0x3B40 - 0x3B52]

table 6-13 illumination PWM registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B40	PULSE1 DELAY	0x10	RW	First Pulse Delay (0 ~ 31) 0x00: -0.5 frame 0x1F: 0.5 frame
0x3B41	PULSE2 DELAY	0x10	RW	Second Pulse Delay (0 ~ 31) 0x00: -0.5 frame 0x1F: 0.5 frame
0x3B42	PULSE3 DELAY	0x10	RW	Third Pulse Delay (0 ~ 31) 0x00: -0.5 frame 0x1F: 0.5 frame
0x3B43	PULSE4 DELAY	0x10	RW	Fourth Pulse Delay (0 ~ 31) 0x00: -0.5 frame 0x1F: 0.5 frame
0x3B44	DURATION CTRL0	0x11	RW	Bit[7:4]: Second pulse duration (0 ~ 15 frames) Bit[3:0]: First pulse duration (0 ~ 15 frames)
0x3B45	DURATION CTRL1	0x11	RW	Bit[7:4]: Fourth pulse duration (0 ~ 15 frames) Bit[3:0]: Third pulse duration (0 ~ 15 frames)
0x3B46	PULSE1 DUTY	0x1F	RW	First Pulse Duty Cycle (0 ~ 31)
0x3B47	PULSE2 DUTY	0x1F	RW	Second Pulse Duty Cycle (0 ~ 31)
0x3B48	PULSE3 DUTY	0x1F	RW	Third Pulse Duty Cycle (0 ~ 31)
0x3B49	PULSE4 DUTY	0x1F	RW	Fourth Pulse Duty Cycle (0 ~ 31)
0x3B4A	GAP1	0x00	RW	Gap B/W Pulse 1 and Pulse 2 (0 ~ 255 Frames)
0x3B4B	GAP2	0x00	RW	Gap B/W Pulse 2 and Pulse 3 (0 ~ 255 Frames)
0x3B4C	GAP3	0x00	RW	Gap B/W Pulse 3 and Pulse 4 (0 ~ 255 Frames)
0x3B4D	GAP4	0x00	RW	Gap B/W Pulse 4 and Pulse 1 (0 ~ 255 Frames)

table 6-13 illumination PWM registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B4E	PWM CTRL	0x00	RW	Bit[7]: pwm_req_r (read only) Bit[6]: dly_option Bit[5]: illum_sel Bit[4]: duty_no_map Bit[3]: no_gap Bit[2]: sel_slot_out Bit[1]: Manually set duty cycle for duration1 and duration 3 Bit[0]: pwm_repeat
0x3B4F	SLOT WIDTH	0x02	RW	Slot Width
0x3B50	PULSE2 DUTY STEP	0x01	RW	ramp2_xstep Second Pulse Duty Cycle Step
0x3B51	PULSE4 DUTY STEP	0x01	RW	ramp4_xstep Fourth Pulse Duty Cycle Step
0x3B52	TAIL_DUTY_CYCLE	0x80	RW	Bit[7]: end_opt 0: No pulse when PWM end 1: Free running at pre-defined duty cycle Bit[6]: tail_stop_toggle Bit[4:0]: duty_tail Tail pulse duty cycle step

6.14 OTP [0x7000 - 0x73FF, 0x3D80 - 0x3D91]

table 6-14 OTP registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x7000~ 0x73FF	OTP_SRAM	0x00	RW	Bit[7:0]: OTP buffer
0x3D80	OTP PROGRAM CTRL	0x00	RW	Bit[7]: otp_pgenb_o 1: Program on going Bit[6:1]: Debug mode Bit[0]: otp_pgm To start program, write 0x1 to this bit

table 6-14 OTP registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3D81	OTP LOAD CTRL	0x00	RW	Bit[7]: opt_load_o 1: Load on going Bit[6:4]: Debug mode Bit[0]: otp_rd (write only) Writing to this register will start data loading
0x3D82	OTP PROGRAM PULSE	0xAA	RW	Bit[7:0]: Control program strobe pulse by 8*Tsclk
0x3D83	OTP LOAD PULSE	0x08	RW	Bit[7:4]: Debug mode Bit[3:0]: Control load strobe pulse, by Tsclk
0x3D84	OPT MODE CTRL	0x80	RW	Bit[7]: program_dis 0: Enable 1: Disable Bit[6]: mode_select 0: Auto mode 1: Manual mode Bit[5:0]: manual_cs
0x3D85	OPT REG85	0x13	RW	Bit[7:3]: Debug mode Bit[2]: OTP powerup load data enable Bit[1]: OTP powerup load setting enable Bit[0]: OTP software load setting enable
0x3D86	OTP SRAM TEST SIGNALS	0x02	RW	Bit[7:6]: Debug mode Bit[5]: r_rme Bit[4]: r_test Bit[3:0]: r_rm
0x3D87	OTP PS2CS	0x0A	RW	Bit[7:4]: Debug mode Bit[3:0]: PS to CSB time control, by SCLK
0x3D88	OTP MANUAL START HIGH ADDR	0x00	RW	Bit[7:0]: Start high address for manual mode
0x3D89	OTP MANUAL START LOW ADDR	0x00	RW	Bit[7:0]: Start low address for manual mode
0x3D8A	OTP MANUAL END HIGH ADDR	0x00	RW	Bit[7:0]: End high address for manual mode
0x3D8B	OTP MANUAL END LOW ADDR	0x00	RW	Bit[7:0]: End low address for manual mode
0x3D8C	OTP LOAD START HIGH ADDR	0x00	RW	Bit[7:0]: Start high address for load setting
0x3D8D	OTP LOAD START LOW ADDR	0x00	RW	Bit[7:0]: Start low address for load setting
0x3D8E~ 0x3D8F	DEBUG MODE	–	–	Debug Mode

table 6-14 OTP registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3D90	OTP STROBE GAP PGM	0x12	RW	Bit[7:0]: Gap between STROBE pulse when program
0x3D91	OTP STROBE GAP LOAD	0x06	RW	Bit[7:4]: Debug mode Bit[3:0]: Gap between STROBE when load

6.15 ADC sync [0x4500 - 0x4502]

table 6-15 ADC sync registers

address	register name	default value	R/W	description
0x4500~ 0x4502	ADC SYNC	–	–	ADC Sync Registers

6.16 MIPI top [0x4800 - 0x4853]

table 6-16 MIPI top registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x4800	MIPI CTRL00	0x04	RW	Bit[7:6]: Not used Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[2:0]: Not used

table 6-16 MIPI top registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x4801	MIPI CTRL01	0x00	RW	Bit[7]: Debug mode Bit[6]: spkt_dt_sel 1: Use dt_spkt as short packet data Bit[5]: first_bit Change clk_lane first bit 0: Output 0x05 1: Output 0x0A Bit[4:2]: Debug mode Bit[1]: LPX_select for PCLK domain 0: Auto calculate t_lpx_p, unit pclk2x cycle 1: Use lpx_p_min[7:0] Bit[0]: Not used
0x4802	MIPI CTRL02	0x00	RW	Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]

table 6-16 MIPI top registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x4803	MIPI CTRL03	0x00	RW	Bit[7:4]: Debug mode Bit[3]: manu_ofset_ot_perio Manual offset SMIA Bit[2]: r_manu_half2one t_period half to 1 SMIA Bit[1:0]: Not used 0: hs_pre_half 1: clk_pre_half
0x4804	MIPI CTRL04	0x04	RW	Bit[7:4]: man_lane_num Bit[3]: lane_num_manual_enable Bit[2]: lane4_6b_en1 Supports 4,7,8-lane 6-bit Bit[1] vsub select 0: Valid in behind 1: Valid in front Bit[0]: Not used Input data valid 0: Valid=8 1: Valid=4
0x4805	MIPI CTRL05	0x00	RW	Bit[7:4]: Debug mode Bit[3]: lpda_retim_manu_o Bit[2]: lpda_retim_sel_o 1: Manual Bit[1]: lpck_retim_manu_o Bit[0]: lpck_retim_sel_o 1: Manual
0x4806	MIPI CTRL06	0x00	RW	Bit[7:5]: Debug mode Bit[4]: pu_mark_en_o Power up mark1 enable Bit[3] mipi_remot_rst Bit[2]: mipi_susp Bit[1] smia_lane_ch_en Bit[0] tx_lsb_first 0: Transmit high bit first 1: Low power transmit low bit first
0x4807	DEBUG MODE	–	–	Debug Mode
0x4808	MIPI CTRL08	0x0A	RW	Bit[7:0]: wkup_dly Mark1 wakeup delay/2^10
0x4810	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[15:8] High byte of max frame counter of frame sync short packet
0x4811	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[7:0] Low byte of max frame counter of frame sync short packet

table 6-16 MIPI top registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x4813	MIPI CTRL13	0x00	RW	Bit[7:3]: Debug mode Bit[2]: vc_sel Input VC or register VC Bit[1:0]: VC Virtual channel of MIPI
0x4814	MIPI CTRL14	0x2A	RW	Bit[7]: Debug mode Bit[6]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data Bit[5:0]: dt_man Manual data type
0x4815	MIPI CTRL15	0x00	RW	Bit[7]: Debug mode Bit[6]: pclk_inv 0: Using falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Using rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[5:0]: manu_dt_short Manual type for short packet
0x4816	EMB DT	0x52	RW	Bit[7:6]: Debug mode Bit[5:0]: emb_dt Manual set embedded data type
0x4817	DEBUG MODE	–	–	Debug Mode
0x4818	HS ZERO MIN	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: hs_zero_min[9:8] High byte of minimum value of hs_zero Unit ns
0x4819	HS ZERO MIN	0x70	RW	Bit[7:0]: hs_zero_min[7:0] Low byte of minimum value of hs_zero hs_zero_real =hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_trail_min[9:8] High byte of minimum value of hs_trail, unit ns
0x481B	HS TRAIL MIN	0x3C	RW	Bit[7:0]: hs_trail_min[7:0] Low byte of minimum value of hs_trail hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o

table 6-16 MIPI top registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x481C	CLK ZERO MIN	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: clk_zero_min[9:8] High byte of minimum value of clk_zero, unit ns
0x481D	CLK ZERO MIN	0x2C	RW	Bit[7:0]: clk_zero_min[7:0] Low byte of minimum value of clk_zero clk_zero_real clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	CLK PREPARE MAX	0x5F	RW	Bit[7:0]: clk_prepare_max[7:0] Maximum value of clk_prepare, unit ns
0x481F	CLK PREPARE MIN	0x26	RW	Bit[7:0]: clk_prepare_min[7:0] Minimum value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK POST MIN	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: clk_post_min[9:8] High byte of minimum value of clk_post, unit ns
0x4821	CLK POST MIN	0x3C	RW	Bit[7:0]: clk_post_min[7:0] Low byte of minimum value of clk_post clk_post_real = clk_post_min_o+ Tui*ui_clk_post_min_o
0x4822	CLK TRAIL MIN	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: clk_trail_min[9:8] High byte of minimum value of clk_trail, unit ns
0x4823	CLK TRAIL MIN	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Low byte of minimum value of clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX P MIN	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: lpx_p_min[9:8] High byte of minimum value of lpx_p, unit ns
0x4825	LPX P MIN	0x32	RW	Bit[7:0] lpx_p_min[7:0] Low byte of minimum value of lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o

table 6-16 MIPI top registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x4826	HS PREPARE MIN	0x32	RW	Bit[7:0]: hs_prepare_min[7:0] Minimum value of hs_prepare, unit ns
0x4827	HS PREPARE MAX	0x55	RW	Bit[7:0]: hs_prepare_max[7:0] Maximum value of hs_prepare hs_prepare_real = hs_prepare_max_o + Tui*ui_hs_prepare_max_o
0x4828	HS EXIT MIN	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: hs_exit_min[9:8] High byte of minimum value of hs_exit, unit ns
0x4829	HS EXIT MIN	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Low byte of minimum value of hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	UI HS ZERO MIN	0x06	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_hs_zero_min[5:0] Minimum UI value of hs_zero, unit UI
0x482B	UI HS TRAIL MIN	0x04	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_hs_trail_min[5:0] Minimum UI value of hs_trail, unit UI
0x482C	UI CLK ZERO MIN	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_clk_zero_min[5:0] Minimum UI value of clk_zero, unit UI
0x482D	UI CLK PREPARE	0x00	RW	Bit[7:4]: ui_clk_prepare_max Maximum UI value of clk_prepare, unit UI Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare, unit UI
0x482E	UI CLK POST MIN	0x34	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_clk_post_min[5:0] Minimum UI value of clk_post, unit UI
0x482F	UI CLK TRAIL MIN	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_clk_trail_min[5:0] Minimum UI value of clk_trail, unit UI

table 6-16 MIPI top registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x4830	UI LPX P MIN	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_lpx_p_min[5:0] Minimum UI value of lpx_p (pclk2x domain), unit UI
0x4831	UI HS PREPARE	0x64	RW	Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepare, unit UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare, unit UI
0x4832	UI HS EXIT MIN	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_hs_exit_min[5:0] Minimum UI value of hs_exit, unit UI
0x4833	CTRL51	0x18	RW	Bit[7:6]: Debug mode Bit[5:0]: mipi_pkt_star_size
0x4836	GLB MODE SEL	0x00	RW	Bit[7:1]: Debug mode Bit[0]: smia_cal_en 0: Use period to calculate 1: Use SMIA bitrate to calculate
0x4837	PCLK PERIOD	0x0A	RW	Bit[7:0]: pclk_period[7:0] Period of pclk2x pclk_div=1, and 1-bit decimal
0x4838	MIPI LP GPIO0	0x00	RW	Bit[7] lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6] lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4] lp_n0_o Bit[3] lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2] lp_dir_man1 0: Input 1: Output Bit[1]: lp_p1_o Bit[0]: lp_n1_o

table 6-16 MIPI top registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x4839	MIPI LP GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o
0x483A~ 0x483B	DEBUG MODE	–	–	Debug Mode
0x483C	MIPI CTRL3C	0x02	RW	Bit[7:4]: Debug mode Bit[3:0]: t_clk_pre Unit pclk2x cycle
0x483D	MIPI LP GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use lp_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1_o Bit[0]: lp_ck_n1_o

table 6-16 MIPI top registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x484A	SEL MIPI CTRL4A	0x3F	RW	Bit[7:6]: Debug mode Bit[5]: slp_lp_pon_man_o Set for power up Bit[4]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck Bit[2]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	SMIA OPTION	0x07	RW	Bit[7:3]: Debug mode Bit[2]: line_st_sel_o 0: Line starts after HREF 1: Line starts after fifo_st Bit[1]: clk_start_sel_o 0: Clock starts after SOF 1: Clock start after reset Bit[0]: sof_sel_o 0: Frame starts after HREF come temp 1: Frame starts after SOF
0x484C	SEL MIPI CTRL4C	0x03	RW	Bit[7]: Debug mode Bit[6]: smia_fcnt_i select Bit[5]: prbs_enable Bit[4]: hs_test_only MIPI high speed only test mode enable Bit[3]: set_frame_cnt_0 Set frame count to inactive mode (keep 0) Bit[2:0]: Debug mode
0x484D	TEST PATTEN DATA	0xB6	RW	Bit[7:0]: test_patten_data[7:0] Data lane test pattern register
0x484E	FE DLY	0x10	RW	Bit[7:0]: r_fe_dly_o Last packet to frame end delay / 2
0x484F	TEST PATTEN CK DATA	0x55	RW	Bit[7:0]: clk_test_patten_reg
0x4850	FCNT	–	R	Bit[7:0]: fcnt[15:8]
0x4851	FCNT	–	R	Bit[7:0]: fcnt[7:0]
0x4852	LCNT	–	R	Bit[7:0]: lcnt[15:8]
0x4853	LCNT	–	R	Bit[7:0]: lcnt[7:0]

6.17 LVDS interface [0x4A00 - 0x4A0F]

table 6-17 LVDS interface registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4A00	LVDS R0	0x2A	RW	Bit[7]: Two sync code enable in lane8 mode Bit[6]: Sync code manual mode enable Bit[5]: Sync code enable when only 1 lane Bit[4]: lvds_pclk_inv Bit[3]: Channel ID enable in sync per lane mode Bit[2]: f value Bit[1]: Save first enable Bit[0]: sync code mode 0: Split 1: Per lane
0x4A02	LVDS DUMMY DATA0	0x0	RW	Bit[7:0]: lvds_dummy_data0[11:8] Dummy data0
0x4A03	LVDS DUMMY DATA0	0x80	RW	Bit[7:0]: lvds_dummy_data0[7:0] Dummy data0
0x4A04	LVDS DUMMY DATA1	0x00	RW	Bit[7:0]: lvds_dummy_data1[11:8] Dummy data1
0x4A05	LVDS DUMMY DATA1	0x10	RW	Bit[7:0]: lvds_dummy_data1[7:0] Dummy data1
0x4A06	LVDS R6	0xAA	RW	Bit[7:0]: lvds_r6 frame_start sync code in manual sync code mode
0x4A07	LVDS R7	0x55	RW	Bit[7:0]: lvds_r7 frame_end sync code in manual sync code mode
0x4A08	LVDS R8	0x99	RW	Bit[7:0]: lvds_r8 line_start sync code in manual sync code mode
0x4A09	LVDS R9	0x66	RW	Bit[7:0]: lvds_r9 line_end sync code in manual sync code mode
0x4A0A	LVDS RA	0x08	RW	Bit[7:3]: Debug mode Bit[2]: r_hts_man_en Bit[1]: r_ln2_sel Bit[0]: r_chk_pcnt

table 6-17 LVDS interface registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4A0B	LVDS SLEEP CTRL	0x88	RW	Bit[7]: sleep_en Bit[4]: frame_rst_en Bit[3:0]: ln_end_dly
0x4A0C	LVDS BLK TIMES	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: lvds_blk_times[11:8]
0x4A0D	LVDS BLK TIMES	0x02	RW	Bit[7:0]: lvds_blk_times[7:0]
0x4A0E	LVDS HTS MAN	0x00	RW	Bit[7:0]: lvds_hts_man[15:8]
0x4A0F	LVDS HTS MAN	0x00	RW	Bit[7:0]: lvds_hts_man[7:0]

6.18 temperature monitor [0x4D00 - 0x4D13]

table 6-18 temperature monitor registers

address	register name	default value	R/W	description
0x4D00~ 0x4D11	DEBUG MODE	–	–	Debug Mode
0x4D12	TPM TRIGGER	0x00	RW	Bit[7:1]: Debug mode Bit[0]: Temperature sensor trigger
0x4D13	TPM READ	–	R	Bit[7:0]: Temperature readout

6.19 LENC [0x5200 - 0x5256]

table 6-19 LENC registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5200	LENC G00	0x10	RW	Bit[7:0]: Control point G00 for luminance compensation
0x5201	LENC G01	0x10	RW	Bit[7:0]: Control point G01 for luminance compensation
0x5202	LENC G02	0x10	RW	Bit[7:0]: Control point G02 for luminance compensation

table 6-19 LENC registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5203	LENC G03	0x10	RW	Bit[7:0]: Control point G03 for luminance compensation
0x5204	LENC G04	0x10	RW	Bit[7:0]: Control point G04 for luminance compensation
0x5205	LENC G05	0x10	RW	Bit[7:0]: Control point G05 for luminance compensation
0x5206	LENC G10	0x10	RW	Bit[7:0]: Control point G10 for luminance compensation
0x5207	LENC G11	0x08	RW	Bit[7:0]: Control point G11 for luminance compensation
0x5208	LENC G12	0x08	RW	Bit[7:0]: Control point G12 for luminance compensation
0x5209	LENC G13	0x08	RW	Bit[7:0]: Control point G13 for luminance compensation
0x520A	LENC G14	0x08	RW	Bit[7:0]: Control point G14 for luminance compensation
0x520B	LENC G15	0x10	RW	Bit[7:0]: Control point G15 for luminance compensation
0x520C	LENC G20	0x10	RW	Bit[7:0]: Control point G20 for luminance compensation
0x520D	LENC G21	0x08	RW	Bit[7:0]: Control point G21 for luminance compensation
0x520E	LENC G22	0x00	RW	Bit[7:0]: Control point G22 for luminance compensation
0x520F	LENC G23	0x00	RW	Bit[7:0]: Control point G23 for luminance compensation
0x5210	LENC G24	0x08	RW	Bit[7:0]: Control point G24 for luminance compensation
0x5211	LENC G25	0x10	RW	Bit[7:0]: Control point G25 for luminance compensation
0x5212	LENC G30	0x10	RW	Bit[7:0]: Control point G30 for luminance compensation
0x5213	LENC G31	0x08	RW	Bit[7:0]: Control point G31 for luminance compensation
0x5214	LENC G32	0x00	RW	Bit[7:0]: Control point G32 for luminance compensation
0x5215	LENC G33	0x00	RW	Bit[7:0]: Control point G33 for luminance compensation

table 6-19 LENC registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x5216	LENC G34	0x08	RW	Bit[7:0]: Control point G34 for luminance compensation
0x5217	LENC G35	0x10	RW	Bit[7:0]: Control point G35 for luminance compensation
0x5218	LENC G40	0x10	RW	Bit[7:0]: Control point G40 for luminance compensation
0x5219	LENC G41	0x08	RW	Bit[7:0]: Control point G41 for luminance compensation
0x521A	LENC G42	0x08	RW	Bit[7:0]: Control point G42 for luminance compensation
0x521B	LENC G43	0x08	RW	Bit[7:0]: Control point G43 for luminance compensation
0x521C	LENC G44	0x08	RW	Bit[7:0]: Control point G44 for luminance compensation
0x521D	LENC G45	0x10	RW	Bit[7:0]: Control point G45 for luminance compensation
0x521E	LENC G50	0x10	RW	Bit[7:0]: Control point G50 for luminance compensation
0x521F	LENC G51	0x10	RW	Bit[7:0]: Control point G51 for luminance compensation
0x5220	LENC G52	0x10	RW	Bit[7:0]: Control point G52 for luminance compensation
0x5221	LENC G53	0x10	RW	Bit[7:0]: Control point G53 for luminance compensation
0x5222	LENC G54	0x10	RW	Bit[7:0]: Control point G54 for luminance compensation
0x5223	LENC G55	0x10	RW	Bit[7:0]: Control point G55 for luminance compensation
0x5224	LENC BR00	0xAA	RW	Bit[7:4]: Control point B00 for blue channel compensation Bit[3:0]: Control point R00 for red channel compensation
0x5225	LENC BR01	0xAA	RW	Bit[7:4]: Control point B01 for blue channel compensation Bit[3:0]: Control point R01 for red channel compensation

table 6-19 LENC registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x5226	LENC BR02	0xAA	RW	Bit[7:4]: Control point B02 for blue channel compensation Bit[3:0]: Control point R02 for red channel compensation
0x5227	LENC BR03	0xAA	RW	Bit[7:4]: Control point B03 for blue channel compensation Bit[3:0]: Control point R03 for red channel compensation
0x5228	LENC BR04	0xAA	RW	Bit[7:4]: Control point B04 for blue channel compensation Bit[3:0]: Control point R04 for red channel compensation
0x5229	LENC BR10	0xAA	RW	Bit[7:4]: Control point B10 for blue channels compensation Bit[3:0]: Control point R10 for red channels compensation
0x522A	LENC BR11	0x99	RW	Bit[7:4]: Control point B11 for blue channels compensation Bit[3:0]: Control point R11 for red channels compensation
0x522B	LENC BR12	0x99	RW	Bit[7:4]: Control point B12 for blue channels compensation Bit[3:0]: Control point R12 for red channels compensation
0x522C	LENC BR13	0x99	RW	Bit[7:4]: Control point B13 for blue channels compensation Bit[3:0]: Control point R13 for red channels compensation
0x522D	LENC BR14	0xAA	RW	Bit[7:4]: Control point B14 for blue channels compensation Bit[3:0]: Control point R14 for red channels compensation
0x522E	LENC BR20	0xAA	RW	Bit[7:4]: Control point B20 for blue channels compensation Bit[3:0]: Control point R20 for red channels compensation
0x522F	LENC BR21	0x99	RW	Bit[7:4]: Control point B21 for blue channels compensation Bit[3:0]: Control point R21 for red channels compensation

table 6-19 LENC registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5230	LENC BR22	0x88	RW	Bit[7:4]: Control point B22 for blue channels compensation Bit[3:0]: Control point R22 for red channels compensation
0x5231	LENC BR23	0x99	RW	Bit[7:4]: Control point B23 for blue channels compensation Bit[3:0]: Control point R23 for red channels compensation
0x5232	LENC BR24	0xAA	RW	Bit[7:4]: Control point B24 for blue channels compensation Bit[3:0]: Control point R24 for red channels compensation
0x5233	LENC BR30	0xAA	RW	Bit[7:4]: Control point B30 for blue channels compensation Bit[3:0]: Control point R30 for red channels compensation
0x5234	LENC BR31	0x99	RW	Bit[7:4]: Control point B31 for blue channels compensation Bit[3:0]: Control point R31 for red channels compensation
0x5235	LENC BR32	0x99	RW	Bit[7:4]: Control point B32 for blue channels compensation Bit[3:0]: Control point R32 for red channels compensation
0x5236	LENC BR33	0x99	RW	Bit[7:4]: Control point B33 for blue channels compensation Bit[3:0]: Control point R33 for red channels compensation
0x5237	LENC BR34	0xAA	RW	Bit[7:4]: Control point B34for blue channels compensation Bit[3:0]: Control point R34 for red channels compensation
0x5238	LENC BR40	0xAA	RW	Bit[7:4]: Control point B40 for blue channels compensation Bit[3:0]: Control point R40 for red channels compensation
0x5239	LENC BR41	0xAA	RW	Bit[7:4]: Control point B41 for blue channels compensation Bit[3:0]: Control point R41 for red channels compensation

table 6-19 LENC registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x523A	LENC BR42	0xAA	RW	Bit[7:4]: Control point B42 for blue channels compensation Bit[3:0]: Control point R4 for red channels compensation
0x523B	LENC BR43	0xAA	RW	Bit[7:4]: Control point B43 for blue channels compensation Bit[3:0]: Control point R43 for red channels compensation
0x523C	LENC BR44	0xAA	RW	Bit[7:4]: Control point B44 for blue channels compensation Bit[3:0]: Control point R44 for red channels compensation
0x523D	LENC BR OFFSET	0x88	RW	Bit[7:4]: Base value for all blue channel control points Bit[3:0]: Base value for all red channel control points
0x523E	MAXGAIN	0x40	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will be the minimum value (min LENC gain). Register value is 16 times sensor gain.
0x523F	MINGAIN	0x20	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will start to decrease; otherwise, the amplitude will not change. Register value is 16 times sensor gain.
0x5240	MINQ	0x18	RW	Bit[7]: Debug mode Bit[6:0]: This value indicates the minimum amplitude which luminance channel compensates when AutoLensSwitchEnable is true. Value should be in the range [0~64]

6.20 test mode [0x3E00 - 0x3E13]

table 6-20 test mode registers

address	register name	default value	R/W	description
0x3E00~ 0x3E13	TEST MODE	–	–	Test Mode Registers

6.21 test mode [0x4300 - 0x430D]

table 6-21 test mode registers

address	register name	default value	R/W	description
0x4300~ 0x430D	TEST MODE	–	–	Test Mode Registers

6.22 ISPFC [0x4240 - 0x4243]

table 6-22 ISPFC registers

address	register name	default value	R/W	description
0x4240	FRAME CTRL0	0x00	RW	Bit[7:3]: Debug mode Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4241	FRAME ON NUMBER	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Frame on number
0x4242	FRAME OFF NUMBER	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Frame off number
0x4243	FRAME CTRL1	0x00	RW	Bit[7:6]: Debug mode Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.23 VFIFO [0x4600 - 0x4604]

table 6-23 VFIFO registers

address	register name	default value	R/W	description
0x4600	R VFIFO READ START	0x00	RW	Bit[7:0]: r_vfifo_read_start[15:8] read_start size
0x4601	R VFIFO READ START	0x04	RW	Bit[7:0]: r_vfifo_read_start[7:0] read_start size
0x4602	R2	0x20	RW	Bit[7:4]: r_rm Bit[3]: r_test1 Bit[2]: Not used Bit[1]: Frame reset enable Bit[0]: RAM bypass enable
0x4603	R3	0x00	RW	Bit[7:2]: Debug mode Bit[1]: sram_rme Bit[0]: man_start_mode
0x4604	R4	–	R	Bit[7:2]: Debug mode Bit[3]: ram_full Bit[2]: ram_empty Bit[1]: fo_full Bit[0]: fo_empty

6.24 ISP window [0x5A00 - 0x5A0C]

table 6-24 ISP window registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5A00	XSTART	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: xstart[11:8] Horizontal start address
0x5A01	XSTART	0x00	RW	Bit[7:0]: xstart[7:0] Horizontal start address
0x5A02	YSTART	0x00	RW	Bit[7:3]: Not used Bit[2:0]: ystart[10:8] Vertical start address
0x5A03	YSTART	0x00	RW	Bit[7:0]: ystart[7:0] Vertical start address

table 6-24 ISP window registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5A04	X WIN	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: x_win[11:8] Select window width
0x5A05	X WIN	0x80	RW	Bit[7:0]: x_win[7:0] Select window width
0x5A06	Y WIN	0x05	RW	Bit[7:3]: Not used Bit[2:0]: y_win[10:8] Select window height
0x5A07	Y WIN	0xF0	RW	Bit[7:0]: y_win[7:0] Select window height
0x5A08	WIN CTRL 08	0x00	RW	Bit[7:0]: win_ctrl_08[7:0] Bit[7:2]: Not used Bit[1]: emb_flag_sel 0: Select top line 1: Select bottom line Bit[0]: win_man_en 0: Window size from window top 1: Window size from register
0x5A09	PX CNT	–	R	Bit[7:4]: Not used Bit[3:0]: px_cnt[11:8] Pixel count from input image in horizontal
0x5A0A	PX CNT	–	R	Bit[7:0]: px_cnt[7:0] Pixel count from input image in horizontal
0x5A0B	LN CNT	–	R	Bit[7:3]: Not used Bit[2:0]: ln_cnt[10:8] Line count from input image in vertical
0x5A0C	LN CNT	–	R	Bit[7:0]: ln_cnt[7:0] Line count from input image in vertical

6.25 DPC [0x5300 - 0x5327]

table 6-25 DPC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5300	R DPC CTRL00	0x1C	RW	Bit[7]: r_tail_en Bit[6]: r_sat_en Bit[5]: r_cluster Bit[4]: r_scon_en Bit[3]: r_dcon_en Bit[2]: r_smooth_en Bit[1]: r_bwsnr_en Bit[0]: r_man_mode_en
0x5301	R DPC CTRL01	0xDF	RW	Bit[7]: r_man_tthre Bit[6]: r_comp_en Bit[5]: r_vertical_bp_en Bit[4]: r_color_line_en Bit[3]: r_single_en Bit[2]: r_tcluster_en Bit[1:0]: r_edge_opt[1:0]
0x5302	R DPC CTRL02	0x3F	RW	Bit[7:6]: Not used Bit[5:4]: r_unsat_cross_num Bit[3:2]: r_unsat_num Bit[1:0]: r_vnum
0x5303	R WTHREGLIST1	0x08	RW	Bit[7]: Not used Bit[6:0]: r_wthreglist1[6:0]
0x5304	R BTHREGLIST2	0x20	RW	Bit[7]: Not used Bit6:0]: r_bthreglist2[6:0]
0x5305	R THRE1	0x10	RW	Bit[7]: Not used Bit[6:0]: r_thre1[6:0]
0x5306	R THRE2	0x20	RW	Bit[7]: Not used Bit[6:0]: r_thre2[6:0]
0x5307	R THRE3	0x10	RW	Bit[7:0]: r_thre3[7:0]
0x5308	R THRE4	0x18	RW	Bit[7]: Not used Bit[6:0]: r_thre4[6:0]
0x5309	R WTHRE LIST0	0x08	RW	Bit[7]: Not used Bit[6:0]: r_wthre_list0[6:0]
0x530A	R WTHRE LIST1	0x04	RW	Bit[7]: Not used Bit[6:0]: r_wthre_list1[6:0]
0x530B	R WTHRE LIST2	0x02	RW	Bit[7]: Not used Bit[6:0]: r_wthre_list2[6:0]
0x530C	R WTHRE LIST3	0x02	RW	Bit[7]: Not used Bit[6:0: r_wthre_list3[6:0]

table 6-25 DPC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x530D	R BTHRE LIST0	0x0C	RW	Bit[7]: Not used Bit[6:0]: r_bthre_list0[6:0]
0x530E	R BTHRE LIST1	0x06	RW	Bit[7]: Not used Bit[6:0]: r_bthre_list1[6:0]
0x530F	R BTHRE LIST2	0x02	RW	Bit[7]: Not used Bit[6:0]: r_bthre_list2[6:0]
0x5310	R BTHRE LIST3	0x02	RW	Bit[7]: Not used Bit[6:0]: r_bthre_list3[6:0]
0x5311	R SAT	0xFF	RW	Bit[7:0: r_sat[7:0]
0x5312	R DPC CTRL12	0x07	RW	Bit[7]: Not used Bit[6:0]: vb_gain_th1
0x5313	R DPC CTRL13	0x03	RW	Bit[7]: Not used Bit[6:0]: vb_gain_th2
0x5314	R DPC CTRL14	0x03	RW	Bit[7]: Not used Bit[6:0]: r_smooth_glist0
0x5315	R DPC CTRL15	0x07	RW	Bit[7]: Not used Bit[6:0]: r_smooth_glist1
0x5316	R DPC CTRL16	0x0F	RW	Bit[7]: Not used Bit[6:0]: r_smooth_glist2
0x5317	R DPC CTRL17	0x07	RW	Bit[7]: Not used Bit[6:0]: r_smgain_th1
0x5318	R DPC CTRL18	0x03	RW	Bit[7]: Not used Bit[6:0]: r_smgain_th2
0x5319	R DPC CTRL19	0xF0	RW	Bit[7:0]: r_unsat
0x531A	R DPC CTRL1A	0x08	RW	Bit[7:0]: r_tthre
0x5320~ 0x5327	DEBUG MODE	–	–	Debug Mode

6.26 color bar / scalar control [0x5E00 - 0x5E01]

table 6-26 color bar/scalar control registers

address	register name	default value	R/W	description
0x5E00	PRE ISP TEST CTRL	0x00	RW	Bit[7]: test_enable Bit[6]: Rolling enable Rolling bar in test mode Bit[5]: Transparent and normal image enable Bit[4]: Debug mode Bit[3:2]: color_bar style 00: Horizontal bar 01: Vertical fading bar 10: Horizontal fading bar 11: Vertical bar Bit[1:0]: Test selection 00: Color bar 01: Random data 10: Square black white 11: Black
0x5E01	PRE ISP WIN	0x41	RW	Bit[7]: Not used Bit[6]: Window cut enable Bit[5]: ISP test Low bits to 0 Bit[4]: Random Random data reset Bit[3:0]: Random seed

7 operating specifications

7.1 absolute maximum ratings

table 7-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 functional temperature

table 7-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +85°C junction temperature
stable image temperature[b]	0°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

7.3 DC characteristics

table 7-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}	supply voltage (digital core)	1.14	1.2	1.26	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
I_{DD-A}	active (operating) current		35		mA
I_{DD-D}			100		mA
I_{DD-IO}			3		mA
$I_{DDS-SCCB}$	standby current[a]		250		µA
$I_{DDS-PWDN}$			250		µA
$I_{DDS-XSHUTDOWN}$			1		µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V, EVDD = 1.2V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[b]	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}	SIOC and SIOD	1.28	1.8	3.0	V

a. standby current is measured at room temperature

b. based on DOVDD = 1.8V

7.4 AC characteristics

table 7-4 AC characteristics

symbol	parameter	min	typ	max	unit
inputs					
f_{CLK}	input clock frequency	6	24	64	MHz
t_{CLK}	input clock period		41.67		ns
$t_{CLK:DC}$	clock duty cycle	45	50	55	%

7.5 timing characteristics

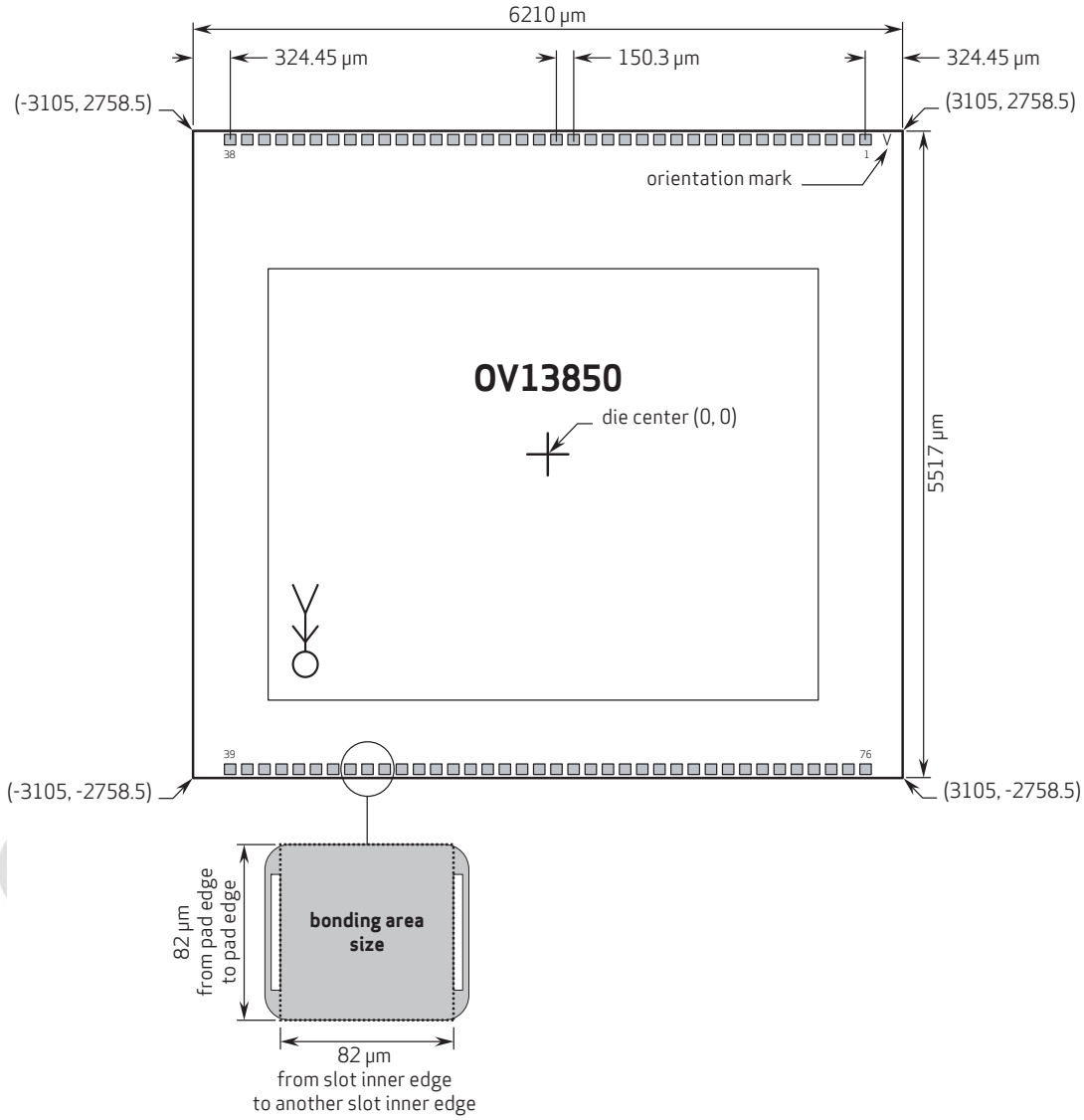
table 7-5 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (EXTCLK)	6	24	64	MHz
t_r, t_f	clock input rise/fall time			TBD	ns

8 mechanical specifications

8.1 COB physical specifications

figure 8-1 COB die specifications



note 1 all dimensions and coordinates are in µm.

note 2 bonding outside the defined area is prohibited as it may cause failue in reliability or functionality 13850_COB_DS_8_1

table 8-1 pad location coordinates (sheet 1 of 3)

pad number	pad name	x coordinate	y coordinate	bonding area size
1	DVDD	2780.55	2683.71	82x82
2	DOGND	2630.25	2683.71	82x82
3	AGND	2479.95	2683.71	82x82
4	AGND	2329.65	2683.71	82x82
5	AVDD	2179.35	2683.71	82x82
6	AVDD	2029.05	2683.71	82x82
7	DVDD	1878.75	2683.71	82x82
8	GPIO1	1728.45	2683.71	82x82
9	SID	1578.15	2683.71	82x82
10	ILPWM	1427.85	2683.71	82x82
11	GPIO	1277.55	2683.71	82x82
12	FSIN	1127.25	2683.71	82x82
13	FREX	976.95	2683.71	82x82
14	DOGND	826.65	2683.71	82x82
15	DOGND	676.35	2683.71	82x82
16	DVDD	526.05	2683.71	82x82
17	DVDD	375.75	2683.71	82x82
18	HREF	225.45	2683.71	82x82
19	SIOD	75.15	2683.71	82x82
20	NC	-75.15	2683.71	82x82
21	SIOC	-225.45	2683.71	82x82
22	NC	-375.75	2683.71	82x82
23	AVDD	-526.05	2683.71	82x82
24	DOVDD	-676.35	2683.71	82x82
25	DOVDD	-826.65	2683.71	82x82
26	DVDD	-976.95	2683.71	82x82
27	DVDD	-1127.25	2683.71	82x82
28	DOGND	-1277.55	2683.71	82x82
29	DOGND	-1427.85	2683.71	82x82
30	ATEST0	-1578.15	2683.71	82x82

table 8-1 pad location coordinates (sheet 2 of 3)

pad number	pad name	x coordinate	y coordinate	bonding area size
31	DOGND	-1728.45	2683.71	82x82
32	DOGND	-1878.75	2683.71	82x82
33	DVDD	-2029.05	2683.71	82x82
34	DVDD	-2179.35	2683.71	82x82
35	AVDD	-2329.65	2683.71	82x82
36	AVDD	-2479.95	2683.71	82x82
37	AGND	-2630.25	2683.71	82x82
38	AGND	-2780.55	2683.71	82x82
39	AGND	-2780.55	-2683.71	82x82
40	AVDD	-2630.25	-2683.71	82x82
41	DOGND	-2479.95	-2683.71	82x82
42	DVDD	-2329.65	-2683.71	82x82
43	VH	-2179.35	-2683.71	82x82
44	VN	-2029.05	-2683.71	82x82
45	DOVDD	-1878.75	-2683.71	82x82
46	XSHUTDOWN	-1728.45	-2683.71	82x82
47	PWDNB	-1578.15	-2683.71	82x82
48	AGND	-1427.85	-2683.71	82x82
49	AVDD	-1277.55	-2683.71	82x82
50	TM	-1127.25	-2683.71	82x82
51	STROBE	-976.95	-2683.71	82x82
52	DOVDD	-826.65	-2683.71	82x82
53	MDP2	-676.35	-2683.71	82x82
54	MDN2	-526.05	-2683.71	82x82
55	EVDD	-375.75	-2683.71	82x82
56	MDP0	-225.45	-2683.71	82x82
57	MDN0	-75.15	-2683.71	82x82
58	EGND	75.15	-2683.71	82x82
59	PVDD	225.45	-2683.71	82x82
60	EGND	375.75	-2683.71	82x82

table 8-1 pad location coordinates (sheet 3 of 3)

pad number	pad name	x coordinate	y coordinate	bonding area size
61	EVDD	526.05	-2683.71	82x82
62	MCP	676.35	-2683.71	82x82
63	MCN	826.65	-2683.71	82x82
64	EGND	976.95	-2683.71	82x82
65	MDP1	1127.25	-2683.71	82x82
66	MDN1	1277.55	-2683.71	82x82
67	EVDD	1427.85	-2683.71	82x82
68	MDP3	1578.15	-2683.71	82x82
69	MDN3	1728.45	-2683.71	82x82
70	DOGND	1878.75	-2683.71	82x82
71	VSYNC	2029.05	-2683.71	82x82
72	EXTCLK	2179.35	-2683.71	82x82
73	DOGND	2329.65	-2683.71	82x82
74	DOGND	2479.95	-2683.71	82x82
75	DVDD	2630.25	-2683.71	82x82
76	DVDD	2780.55	-2683.71	82x82

8.2 reconstructed wafer (RW) physical specifications

- maximum total die count: 621
- film frame: Compact Disco Stainless SUS420
- carrier tape: UV tape

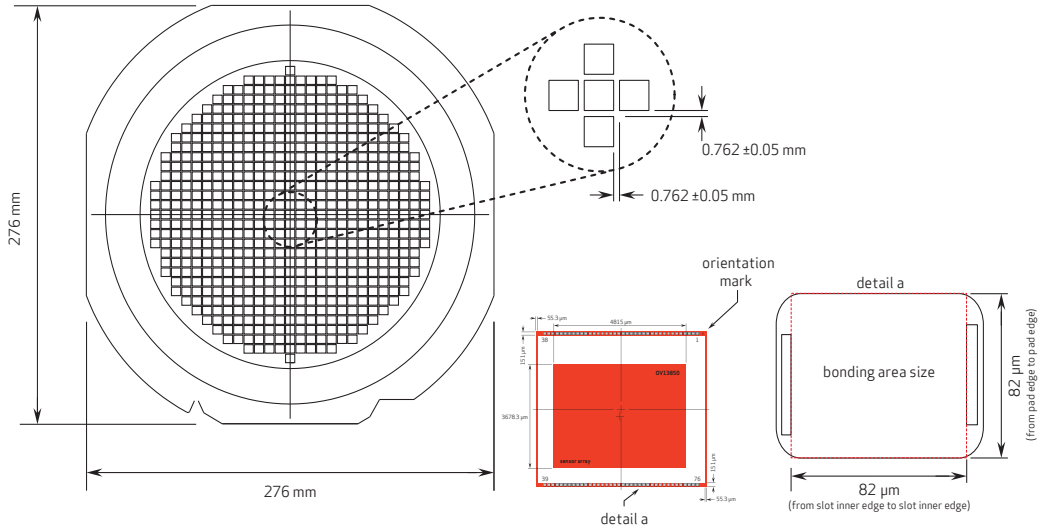
table 8-2 RW physical dimensions

feature	dimensions
RW physical dimensions	8" RW on 12" frame
wafer thickness (OVXXXXX-ABCD)	
C=4	200 µm ± 10 µm (7.9 mil ± 0.4 mil)
reconstructed wafer street width	0.762 mm (30 mil) ± 0.05 mm
placement accuracy x, y, theta	± 50 µm (± 2 mil), <1.0 degree
singulated die size	
width	6260 µm ± 20 µm (246.5 mil ± 0.8 mil)
length	5567 µm ± 20 µm (219 mil ± 0.8 mil)
bond pad size	96 µm × 82 µm (3.8 mil × 3.2 mil)
minimum bond pad pitch	150.3 µm (5.9 mil)
bonding area size	82 µm × 82 µm (3.2 mil × 3.2 mil)
optical array	
die center	(0, 0)
optical center from die center[a]	-40.5 µm, -255.6 µm (-1.6 mil, -10.1 mil)

a. based on die orientation on frame with notch facing down position

note
Actual die count varies and the absent die may be less than 10% of the maximum total die count (excluding the last frame of the wafer lot).

figure 8-2 OV13850 RW physical diagram



note 1 bonding outside the defined bonding area is prohibited, it may potentially induce reliablity issues or functionality failure

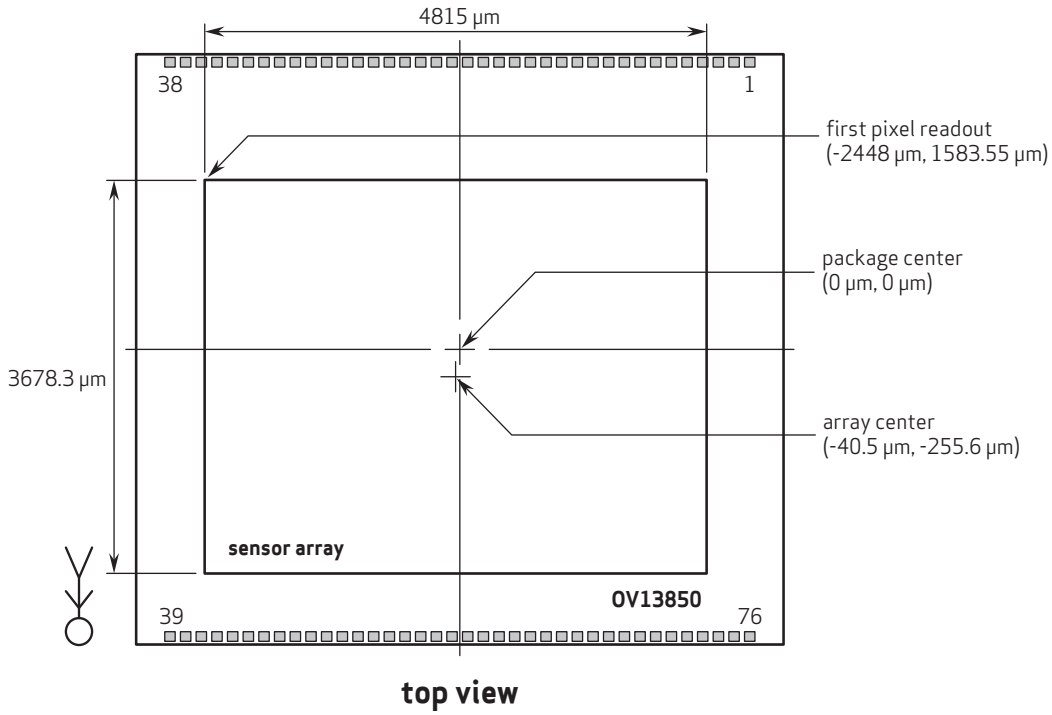
note 2 keep-out-of-contact areas are highlighted in red color for related process fixtures/tools (e.g., nozzle, collets, etc.)

13850_COB_DS_8_2

9 optical specifications

9.1 sensor array center

figure 9-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pad 1 oriented down on the PCB.

13850_COB_DS_9_1

9.2 lens chief ray angle (CRA)

figure 9-2 chief ray angle (CRA)

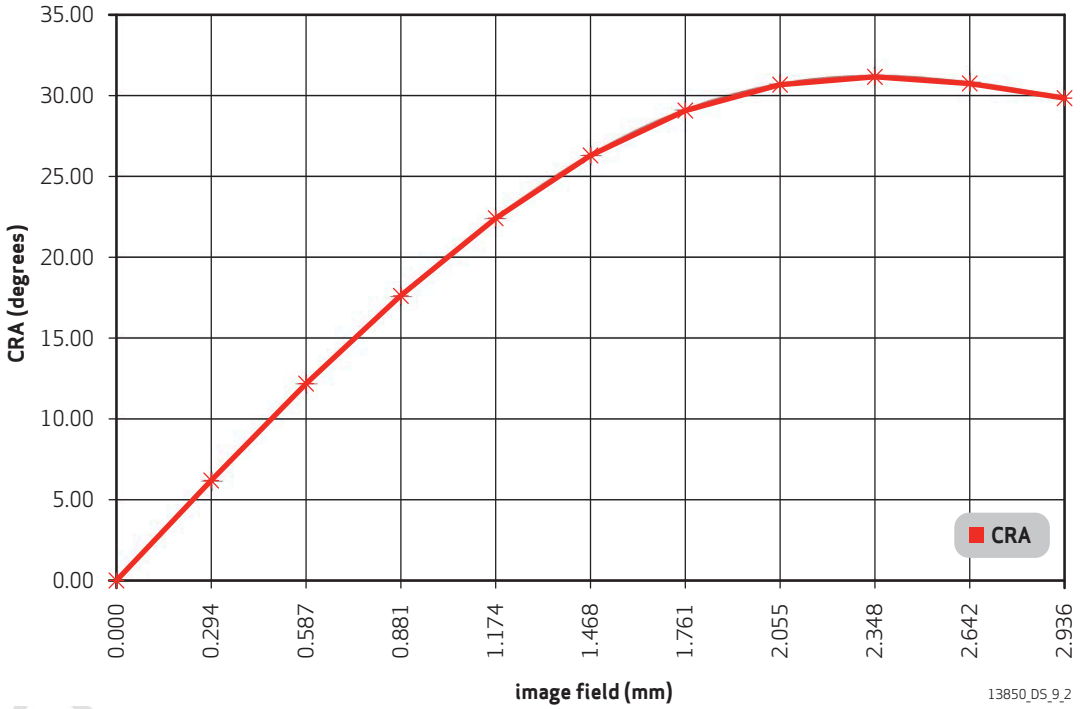


table 9-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.00
0.10	0.294	6.20
0.20	0.587	12.20
0.30	0.881	17.60
0.40	1.174	22.40
0.50	1.468	26.30
0.60	1.761	29.10
0.70	2.055	30.70
0.80	2.348	31.20
0.90	2.642	30.80
1.00	2.936	29.90

appendix A handling of RW devices

A.1 ESD /EOS prevention

1. Ensure that there is 500V ESD control in all work areas.
2. Use ESD safety shoes, ground strap, and static control smocks in test areas.
3. Use grounded work carts and tables in inspection areas.
4. OmniVision recommends the use of ionized air in all work areas.

A.2 particles and cleanliness of environment

1. All production, inspection and packaging areas should meet Class10 environment requirements.
2. Use optical microscopes with 50X and 100X magnifications for particle inspection.
3. Ensure that there is good cassette sealing for particle protection during storage.
4. OmniVision recommends air blowing to remove removable particles.
5. RW die should be stored in nitrogen gas purged cabinets with temperature less than 30°C and relative humidity of 60% before assembly.

A.3 other requirements

1. Reliability assurance of RW or COB bare die is certified by product reliability of the bare die in a CLCC, CSP or QFP package form factor. Precautions should be taken if the packaging form factor of the bare die is other than these specified.
2. Avoid exposure to strong sunlight for extended periods of time as the color filter of the image sensor may become discolored.
3. Avoid direct exposure of the sensor bare die to high temperature and/or humidity environment as sensor characteristics will be affected. Extra precautions should be exercised if the bare die experiences temperatures exceeding 260°C for more than 75 seconds.

revision history

version 1.0 05.24.2013

- initial release

version 1.01 08.21.2013

- in section 8.2, changed carrier tape from "FSL-N6600" to "UV tape"

version 1.1 09.18.2013

- in key specifications, changed power requirements to 223mW (active), 300µW (standby), and 1µW (XSHUTDOWN)
- in chapter 4, removed subsection 4.7.2
- in table 6-1, changed bit description for 0x3012[7:4] to "0000: 0 lane; 0001: 1 lane; 0010: 2 lanes; 0100: 4 lanes"
- in table 7-3, changed typ values for active current to 35mA (I_{DD-A}) and 3mA (I_{DD-IO}) and added typ value 100mA for active current (I_{DD-D})
- in table 7-3, changed typ values for standby current to 250µA ($I_{DDS-SCCB}$), 250µA ($I_{DDS-PWDN}$), and 1µA ($I_{DDS-XSHUTDOWN}$)

version 1.2 10.22.2013

- in features, removed reference to frame exposure mode and added sidebar note
- in table 1-1, removed "(internal pull down resistor)" from pad 9 description
- in table 1-3, moved SID to new row
- in section 2, updated figures 2-3, 2-4, and 2-5
- in table 4-3, changed description for register bit 0x4000[4] to "Not used"
- in section 4.7, removed second paragraph from sub-section 4.7.1.4, table 4-8 and sub-sections 4.7.1.5~4.7.1.10
- in section 5.1, removed RAW scalar from section description
- in section 6, changed "... 0x6C for write and 0x61 for read..." to "... 0x6C for write and 0x6D..." and removed section 6.6
- in table 6-11, changed description for register bit 0x4000[4] to "Not used"
- in table 7-3, removed "for 2-lane MIPI..." from V_{DD-D} parameter and changed "I_{DDB}" to "I_{DDS}" for standby current symbols

defining the future of digital imaging™

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