SONY

Diagonal 5.7 mm (Type 1/3.2) CMOS Image Sensor with Square Pixel for Color Cameras

IMX179QQH5-C

Description

The IMX179 is a diagonal 5.7 mm (Type 1/3.2) CMOS active pixel type image sensor with a square pixel array and 8.08M effective pixels. This chip operates with three power supplies, analogue 2.7 V, digital 1.2 V, and IF 1.8 V, and has low power consumption. High sensitivity, low dark current, and no smear are achieved through the adoption of R, G, and B primary color pigment mosaic filters. This chip features an electronic shutter with variable charge-storage time.
In addition, this product is designed for use in cellular phone and tablet PC. When using this for another application, Sony does not guarantee the quality and reliability of product.
Therefore, don't use this for applications other than cellular phone and tablet PC. Consult your Sony sales representative if you have any questions.

Features

- ◆CMOS active pixel type dots
- ◆2-wire serial communication circuit on chip
- ◆CSI2 serial data output
- ◆Timing generator, H and V driver circuits on chip
- ◆CDS/PGA on chip
- ◆10-bit A/D converter on chip
- ◆Automatic optical black (OB) clamp circuit on chip
- ◆PLL on chip (rectangular wave/sine wave)
- ◆High sensitivity, low dark current, no smear
- ◆Excellent anti-blooming characteristics
- ◆Variable-speed shutter function (1H units)
- ◆R, G, B primary color pigment mosaic filters on chip
- ◆Max. 30 frame/s in all-pixel scan mode
- ◆Pixel rate: >260 MHz (>30 frame/s at All-pixel mode)

Exmor R™

* "Exmor R" is a trademark of Sony Corporation. The "Exmor R" is a Sony's CMOS image sensor with significantly enhanced imaging characteristics including sensitivity and low noise by changing fundamental structure of "Exmor" pixel adopted column parallel A/D converter to back-illuminated type.

E13205G42

Device Structure

- ◆CMOS image sensor
- ◆Image size : Diagonal 5.7 mm (Type 1/3.2)
- ◆Total number of pixels : 3288 (H) × 2512 (V) approx. 8.26M pixels
- ◆Number of effective pixels : 3280 (H) × 2464 (V) approx. 8.08M pixels
- ◆Chip size : 6.18 mm (H) × 5.85 mm (V)
- ◆Unit cell size : 1.4µm (H) × 1.4µm (V)
- ◆Substrate material : Silicon

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1-1 Block Diagram

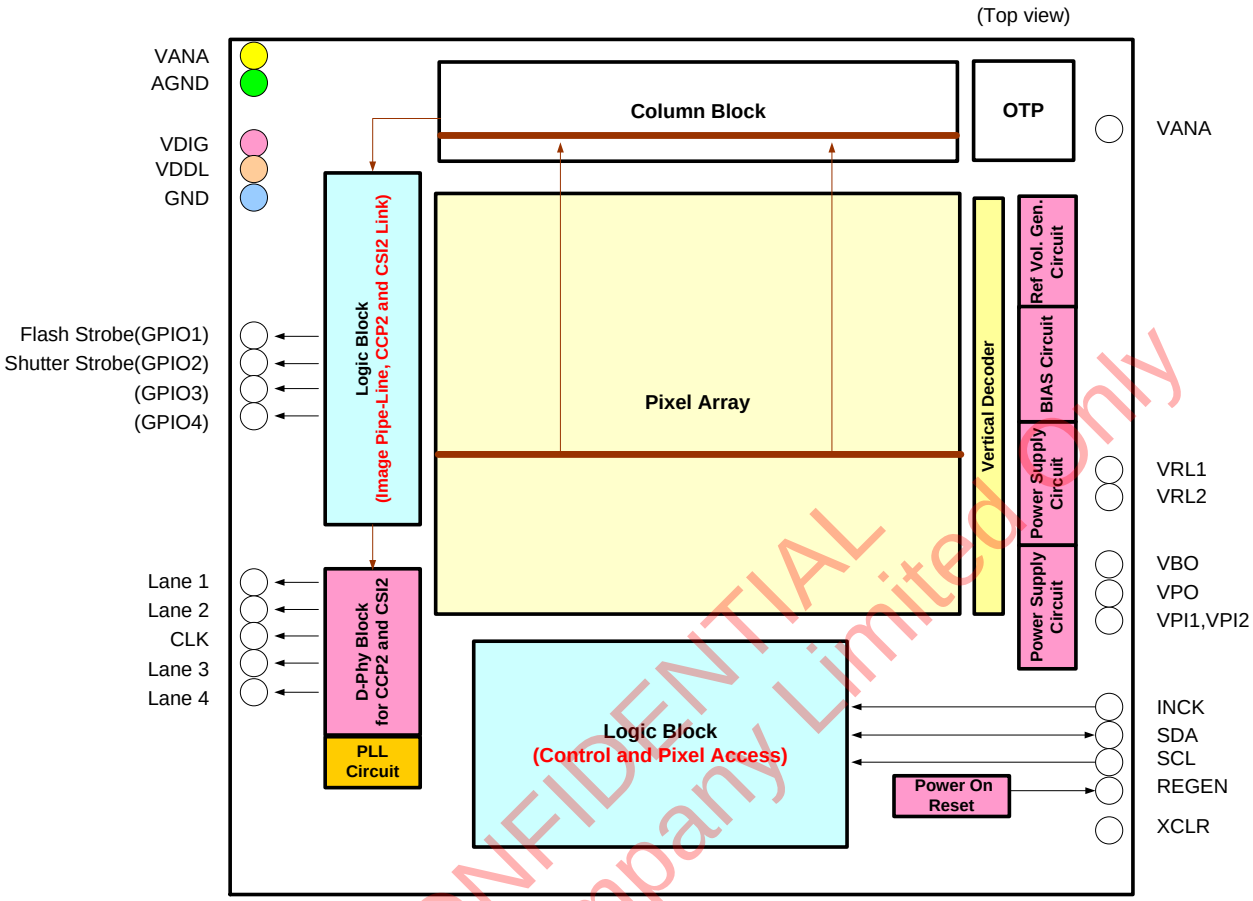


Fig. 1 Block Diagram

1-2 Pin Description

Table. 1 Pin Description

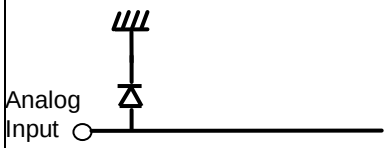
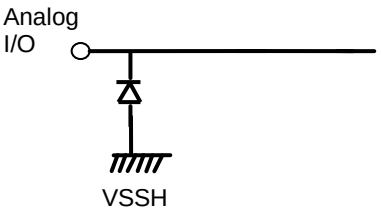
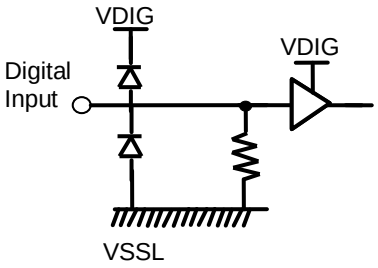
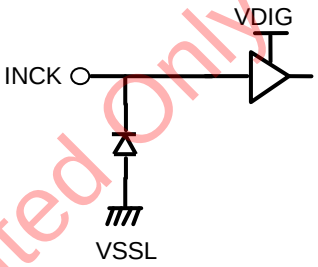
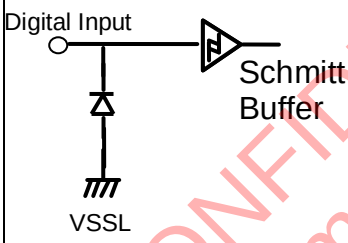
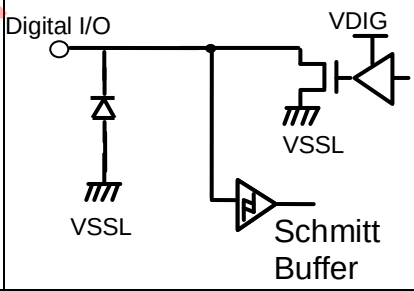
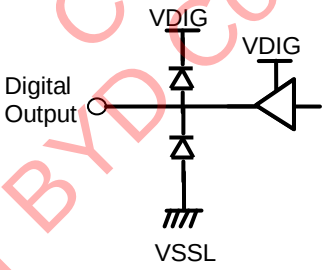
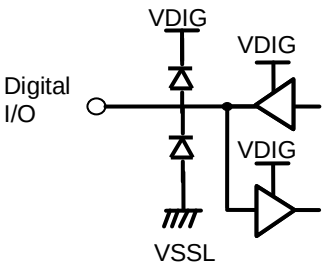
Pin No.	Symbol	I/O	A/D	Description	Remarks
1	VDDLCN1	Power	D	1.2 V power supply	
2	VSSLCN1	GND	D	1.2 V GND	
3	VDDLSC1	Power	D	1.2 V power supply	
4	VSSLSC1	GND	D	1.2 V GND	
5	VDDHCM1	Power	A	2.7 V power supply	
6	VSSHCM1	GND	A	2.7 V GND	
7	VBO	Power	A	Analog output	
8	VPO	Power	A	Analog output	Connect VPI1, VPI2
9	VRL1	O	A	Analog output	
10	VRL2	O	A	Analog output	
11	VSSHCP	GND	A	2.7 V GND	
12	VDDHCP	Power	A	2.7 V power supply	
13	VSSHSN1	GND	A	2.7 V GND	
14	VPI1	I	A	Analog input	Connect VPO, VPI2
15	VDDHSN1	Power	A	2.7 V power supply	
16	VDDSUBD	Power	A	2.7 V power supply	
17	VDDLIO1	Power	D	1.2 V power supply	
18	VSSLIO1	GND	D	1.2 V GND	
19	DMO3P	O	D	CSI2 output	default: GND
20	DMO3N	O	D	CSI2 output	default: GND
21	DMO1P	O	D	CSI2 output	default: GND
22	DMO1N	O	D	CSI2 output	default: GND
23	VSSLIO2	GND	D	1.2 V GND	
24	DCKP	O	D	CSI2 output	default: GND
25	DCKN	O	D	CSI2 output	default: GND
26	VSSLIO3	GND	D	1.2 V GND	
27	DMO2P	O	D	CSI2 output	default: GND
28	DMO2N	O	D	CSI2 output	default: GND
29	DMO4P	O	D	CSI2 output	default: GND
30	DMO4N	O	D	CSI2 output	default: GND
31	VSSLIO4	GND	D	1.2 V GND	
32	VDDLIO2	Power	D	1.2 V power supply	
33	VDDLSC2	Power	D	1.2 V power supply	
34	VSSLSC2	GND	D	1.2 V GND	
35	VSSHPL	GND	A	2.7 V GND	
36	VDDHPL	Power	A	2.7 V power supply	
37	VSSLDM1	GND	D	Dummy PAD	Recommended to be NC

Pin No.	Symbol	I/O	A/D	Description	Remarks
38	VSSLDM2	GND	D	Dummy PAD	↑
39	VSSLDM3	GND	D	Dummy PAD	↑
40	VSSLDM4	GND	D	Dummy PAD	↑
41	VSSLDM5	GND	D	Dummy PAD	↑
42	VSSLDM6	GND	D	Dummy PAD	↑
43	VSSLDM7	GND	D	Dummy PAD	↑
44	VSSLDM8	GND	D	Dummy PAD	↑
45	VSSLDM9	GND	D	Dummy PAD	↑
46	VSSLDM10	GND	D	Dummy PAD	↑
47	VSSLDM11	GND	D	Dummy PAD	↑
48	VSSLDM12	GND	D	Dummy PAD	↑
49	VSSLDM13	GND	D	Dummy PAD	↑
50	VSSLDM37	GND	D	Dummy PAD	↑
51	VSSLDM38	GND	D	Dummy PAD	↑
52	VSSLDM39	GND	D	Dummy PAD	↑
53	VSSLDM40	GND	D	Dummy PAD	↑
54	VSSLDM41	GND	D	Dummy PAD	↑
55	VSSLDM42	GND	D	Dummy PAD	↑
56	VSSLDM43	GND	D	Dummy PAD	↑
57	VSSLDM44	GND	D	Dummy PAD	↑
58	VSSLDM45	GND	D	Dummy PAD	↑
59	VSSLDM46	GND	D	Dummy PAD	↑
60	VSSLDM47	GND	D	Dummy PAD	↑
61	VSSLDM48	GND	D	Dummy PAD	↑
62	VSSLDM49	GND	D	Dummy PAD	↑
63	VDDHFIL	Power	A	2.7 V power supply	connect to 2.7 V power supply
64	VSSLSC3	GND	D	1.2 V GND	
65	VDDLSC3	Power	D	1.2 V power supply	
66	VSSLSC4	GND	D	1.2 V GND	
67	VDDLSC4	Power	D	1.2 V power supply	
68	TENABLE	I	D	1.2 V GND	NC
69	GPIO1	I/O	D	digital input/output	Flash Strobe; default: GND (It is used as Input in Test mode)
70	GPIO2	I/O	D	digital input/output	Shutter Strobe; default: GND (It is used as Input in Test mode)
71	TSCANEN	I	D	digital input	NC
72	GPIO3	O	D	digital output	Internal test use

Pin No.	Symbol	I/O	A/D	Description	Remarks
73	GPIO4	O	D	digital output	Internal test use
74	TEST	I	D	digital input	NC
75	SCL	I	D	digital input	
76	SDA	I/O	D	digital input/output	
77	INCK	I	D	digital input	
78	VDDMCO	Power	D	1.8 V power supply	Noted as "VDIG"
79	POREN	I	D	digital input	NC
80	XCLR	I	D	digital input	Shutdown pin (low active)
81	XPORCD	I	D	digital input	NC
82	REGEN	O	D	digital output	default: GND, In case LDO is inside module
83	TVCDSINP	I	A	analog input	NC
84	TVMON	O	A	analog output	NC
85	VSSHAN	GND	A	2.7 V GND	
86	VDDHAN	Power	A	2.7 V power supply	
87	VSSHSN2	GND	A	2.7 V GND	
88	VPI2	Power	A	Analog input	Connect VPO, VPI1
89	VDDHSN2	Power	A	2.7 V power supply	
90	VSSHCM2	GND	A	2.7 V GND	
91	VDDHCM2	Power	A	2.7 V power supply	
92	VSSLCN2	GND	D	1.2 V GND	
93	VDDLCN2	Power	D	1.2 V power supply	
94	VSSLDM50	GND	D	Dummy PAD	Recommended to be NC
95	VSSLDM51	GND	D	Dummy PAD	↑
96	VSSLDM52	GND	D	Dummy PAD	↑
97	VSSLDM53	GND	D	Dummy PAD	↑
98	VSSLDM54	GND	D	Dummy PAD	↑
99	VSSLDM55	GND	D	Dummy PAD	↑
100	VSSLDM56	GND	D	Dummy PAD	↑
101	VSSLDM57	GND	D	Dummy PAD	↑
102	VSSLDM58	GND	D	Dummy PAD	↑
103	VSSLDM59	GND	D	Dummy PAD	↑
104	VSSLDM60	GND	D	Dummy PAD	↑
105	VSSLDM61	GND	D	Dummy PAD	↑
106	VSSLDM62	GND	D	Dummy PAD	↑
107	VSSLDM63	GND	D	Dummy PAD	↑
108	VSSLDM64	GND	D	Dummy PAD	↑
109	VSSLDM65	GND	D	Dummy PAD	↑

Pin No.	Symbol	I/O	A/D	Description	Remarks
110	VSSLDM66	GND	D	Dummy PAD	↑
111	VSSLDM67	GND	D	Dummy PAD	↑
112	VSSLDM68	GND	D	Dummy PAD	↑
113	VSSLDM69	GND	D	Dummy PAD	↑
114	VSSLDM70	GND	D	Dummy PAD	↑
115	VSSLDM71	GND	D	Dummy PAD	↑
116	VSSLDM72	GND	D	Dummy PAD	↑
117	VSSLDM73	GND	D	Dummy PAD	↑
118	VSSLDM74	GND	D	Dummy PAD	↑
119	VSSLDM75	GND	D	Dummy PAD	↑
120	VSSLDM76	GND	D	Dummy PAD	↑
121	VSSLDM77	GND	D	Dummy PAD	↑
122	VSSLDM78	GND	D	Dummy PAD	↑
123	VSSLDM79	GND	D	Dummy PAD	↑
124	VSSLDM80	GND	D	Dummy PAD	↑
125	VSSLDM81	GND	D	Dummy PAD	↑
126	VSSLDM82	GND	D	Dummy PAD	↑
127	VSSLDM83	GND	D	Dummy PAD	↑
128	VSSLDM84	GND	D	Dummy PAD	↑
129	VSSLDM85	GND	D	Dummy PAD	↑
130	VSSLDM86	GND	D	Dummy PAD	↑
131	VSSLDM87	GND	D	Dummy PAD	↑
132	VSSLDM88	GND	D	Dummy PAD	↑
133	VSSLDM89	GND	D	Dummy PAD	↑
134	VSSLDM90	GND	D	Dummy PAD	↑
135	VSSLDM91	GND	D	Dummy PAD	↑
136	VSSLDM92	GND	D	Dummy PAD	↑
137	VSSLDM93	GND	D	Dummy PAD	↑
138	VSSLDM94	GND	D	Dummy PAD	↑
139	VSSLDM95	GND	D	Dummy PAD	↑
140	VSSLDM96	GND	D	Dummy PAD	↑
141	VSSLDM97	GND	D	Dummy PAD	↑
142	VSSLDM98	GND	D	Dummy PAD	↑

1-3 Pin Equivalent Circuit

Symbol	Equivalent circuit	Symbol	Equivalent circuit
VRL1 VRL2		VPI1 VPI2 VBO VPO	
XCLR		INCK	
SCL		SDA	
REGEN GPIO3 GPIO4		GPIO1 GPIO2	

VDDH: 2.7 V power supply, VDIG: 1.8 V power supply, VDDL: 1.2 V power supply
VSSH: 2.7 V GND, VSSL: 1.2 V GND

Fig. 2 Pin Equivalent Circuit

1-4 Chip Center, Optical Center and Pin Assignment

(Unit: µm)

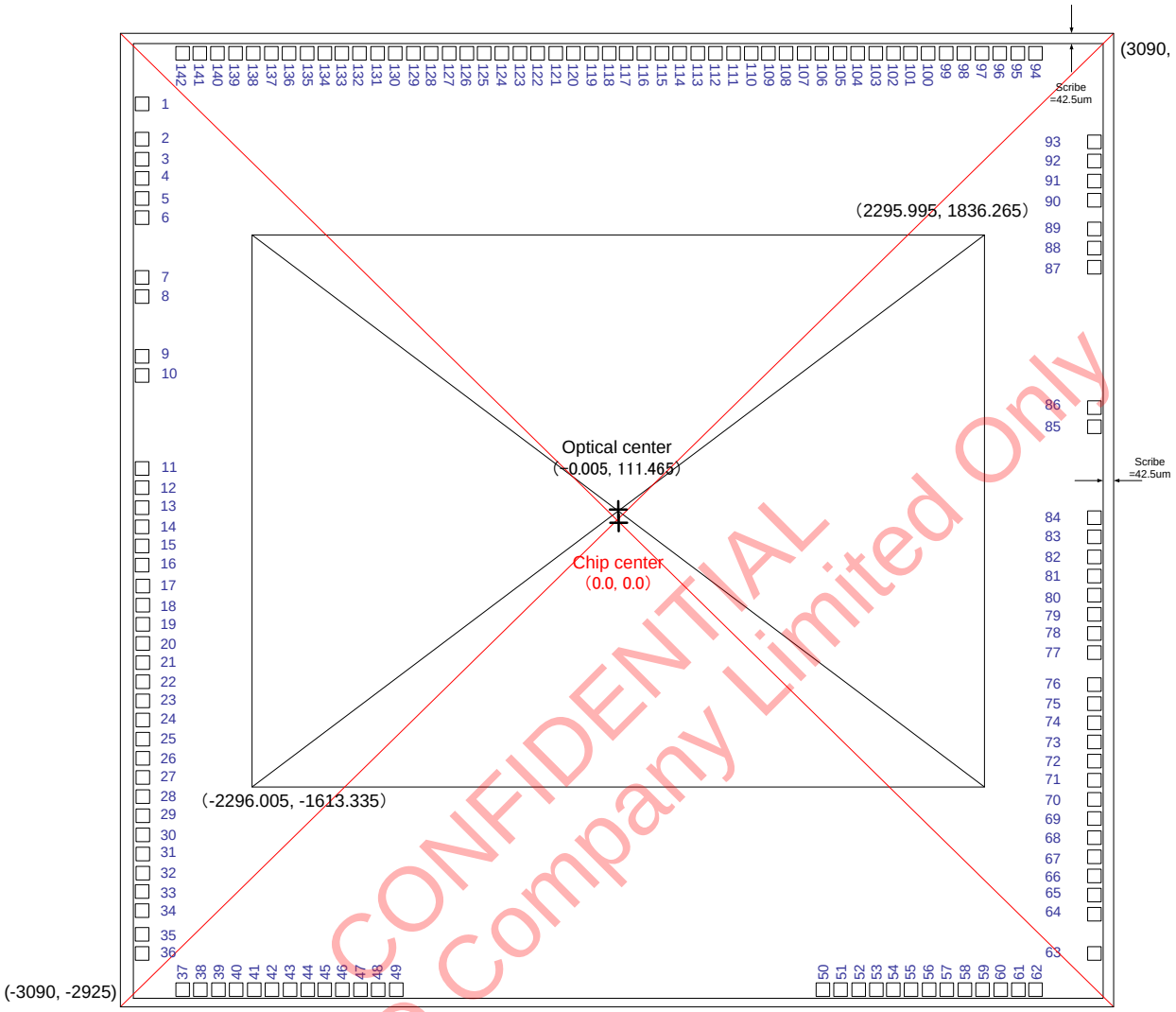


Fig. 3 Chip Center and Optical Center

Chip size 6.18 mm (H) × 5.85 mm (V) contains scribe lines.

1-5 Pin Coordinates

Table. 2 Pin Coordinates

Pin No.	Symbol	X (pad center)	Y (pad center)
1	VDDLCN1	-2952.5	2663.5
2	VSSLCN1	-2992.5	2442.5
3	VDDLSC1	-2992.5	2316.5
4	VSSLSC1	-2992.5	2196.5
5	VDDHCM1	-2992.5	2070.5
6	VSSHCM1	-2992.5	1950.5
7	VBO	-2992.5	1569.7
8	VPO	-2992.5	1449.7
9	VRL1	-2992.5	1074.9
10	VRL2	-2992.5	954.9
11	VSSHCP	-2992.5	371.9
12	VDDHCP	-2992.5	251.9
13	VSSHSN1	-2992.5	125.9
14	VPI1	-2992.5	5.9
15	VDDHSN1	-2992.5	-114.1
16	VDDSUBD	-2992.5	-234.1
17	VDDLIO1	-2992.5	-360.1
18	VSSLIO1	-2992.5	-480.1
19	DMO3P	-2992.5	-600.1
20	DMO3N	-2992.5	-720.1
21	DMO1P	-2992.5	-840.1
22	DMO1N	-2992.5	-960.1
23	VSSLIO2	-2992.5	-1080.1
24	DCKP	-2992.5	-1200.1
25	DCKN	-2992.5	-1320.1
26	VSSLIO3	-2992.5	-1440.1
27	DMO2P	-2992.5	-1560.1
28	DMO2N	-2992.5	-1680.1
29	DMO4P	-2992.5	-1800.1
30	DMO4N	-2992.5	-1920.1
31	VSSLIO4	-2992.5	-2040.1
32	VDDLIO2	-2992.5	-2160.1
33	VDDLSC2	-2992.5	-2280.1
34	VSSLSC2	-2992.5	-2400.1
35	VSSHPL	-2992.5	-2542.5
36	VDDHPL	-2992.5	-2662.5
37	VSSLDM1	-2880	-2827.5
38	VSSLDM2	-2760	-2827.5
39	VSSLDM3	-2640	-2827.5
40	VSSLDM4	-2520	-2827.5
41	VSSLDM5	-2400	-2827.5
42	VSSLDM6	-2280	-2827.5
43	VSSLDM7	-2160	-2827.5
44	VSSLDM8	-2040	-2827.5
45	VSSLDM9	-1920	-2827.5
46	VSSLDM10	-1800	-2827.5
47	VSSLDM11	-1680	-2827.5
48	VSSLDM12	-1560	-2827.5
49	VSSLDM13	-1440	-2827.5
50	VSSLDM37	1440	-2827.5
51	VSSLDM38	1560	-2827.5
52	VSSLDM39	1680	-2827.5
53	VSSLDM40	1800	-2827.5
54	VSSLDM41	1920	-2827.5
55	VSSLDM42	2040	-2827.5
56	VSSLDM43	2160	-2827.5
57	VSSLDM44	2280	-2827.5
58	VSSLDM45	2400	-2827.5
59	VSSLDM46	2520	-2827.5
60	VSSLDM47	2640	-2827.5
61	VSSLDM48	2760	-2827.5
62	VSSLDM49	2880	-2827.5
63	VDDHFIL	2992.5	-2662.5
64	VSSLSC3	2992.5	-2416.5
65	VDDLSC3	2992.5	-2296.5
66	VSSLSC4	2992.5	-2176.5
67	VDDLSC4	2992.5	-2056.5
68	TENABLE	2992.5	-1936.5
69	GPIO1	2992.5	-1816.5
70	GPIO2	2992.5	-1696.5
71	TMASTER	2992.5	-1576.5
72	GPIO3	2992.5	-1456.5

Pin No.	Symbol	X (pad center)	Y (pad center)
73	GPIO4	2992.5	-1336.5
74	TEST	2992.5	-1216.5
75	SCL	2992.5	-1096.5
76	SDA	2992.5	-976.5
77	INCK	2992.5	-776.5
78	VDDMCO	2992.5	-656.5
79	POREN	2992.5	-536.5
80	XCLR	2992.5	-416.5
81	XPORCD	2992.5	-296.5
82	REGEN	2992.5	-176.5
83	TVCDSINP	2992.5	-50.5
84	TVMON	2992.5	69.5
85	VSSHAN	2992.5	639.5
86	VDDHAN	2992.5	759.5
87	VSSHSN2	2992.5	1639.5
88	VPI2	2992.5	1759.5
89	VDDHSN2	2992.5	1879.5
90	VSSHCM2	2992.5	2059.5
91	VDDHCM2	2992.5	2179.5
92	VSSLCN2	2992.5	2305.5
93	VDDLCN2	2992.5	2425.5
94	VSSLDM50	2880	2827.5
95	VSSLDM51	2760	2827.5
96	VSSLDM52	2640	2827.5
97	VSSLDM53	2520	2827.5
98	VSSLDM54	2400	2827.5
99	VSSLDM55	2280	2827.5
100	VSSLDM56	2160	2827.5
101	VSSLDM57	2040	2827.5
102	VSSLDM58	1920	2827.5
103	VSSLDM59	1800	2827.5
104	VSSLDM60	1680	2827.5
105	VSSLDM61	1560	2827.5
106	VSSLDM62	1440	2827.5
107	VSSLDM63	1320	2827.5
108	VSSLDM64	1200	2827.5

Pin No.	Symbol	X (pad center)	Y (pad center)
109	VSSLDM65	1080	2827.5
110	VSSLDM66	960	2827.5
111	VSSLDM67	840	2827.5
112	VSSLDM68	720	2827.5
113	VSSLDM69	600	2827.5
114	VSSLDM70	480	2827.5
115	VSSLDM71	360	2827.5
116	VSSLDM72	240	2827.5
117	VSSLDM73	120	2827.5
118	VSSLDM74	0	2827.5
119	VSSLDM75	-120	2827.5
120	VSSLDM76	-240	2827.5
121	VSSLDM77	-360	2827.5
122	VSSLDM78	-480	2827.5
123	VSSLDM79	-600	2827.5
124	VSSLDM80	-720	2827.5
125	VSSLDM81	-840	2827.5
126	VSSLDM82	-960	2827.5
127	VSSLDM83	-1080	2827.5
128	VSSLDM84	-1200	2827.5
129	VSSLDM85	-1320	2827.5
130	VSSLDM86	-1440	2827.5
131	VSSLDM87	-1560	2827.5
132	VSSLDM88	-1680	2827.5
133	VSSLDM89	-1800	2827.5
134	VSSLDM90	-1920	2827.5
135	VSSLDM91	-2040	2827.5
136	VSSLDM92	-2160	2827.5
137	VSSLDM93	-2280	2827.5
138	VSSLDM94	-2400	2827.5
139	VSSLDM95	-2520	2827.5
140	VSSLDM96	-2640	2827.5
141	VSSLDM97	-2760	2827.5
142	VSSLDM98	-2880	2827.5

2. Pixel Signal Output Specifications

IMX179 has CSI-2 interface and the options are 2 lanes or 4 lanes.

2-1 CSI-2 Signalling Mode

2-1.1 MIPI Transmitter

Output pins (DMO1P/DMO1N, DMO2P/DMO2N, DCKP/DCKN,) of CSI-2 are shown below

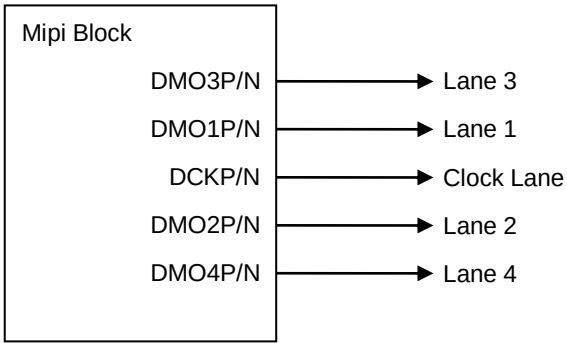


Fig. 4 Relationship between Output pin name and Mipi output Lane

Data and clock signals are transmitted using CSI-2 interface (high speed serial interface). Detailed explanation of CSI-2 interface is in following two documents, “MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) Version 1.00” and “MIPI Alliance Specification for D-PHYVersion 0.90.00”. In CSI-2 interface, one bit of data is transmitted by a pair of differential signals. In the transmitter of CSI-2 interface, differential digital signals of data or clock are converted to differential current signals. At the receiver of CSI-2 interface, inserting output resistance, which is serial to a pair of differential outputs (data or clock), or connecting the receiver block, which includes internal resistance for a pair of differential outputs (data or clock), is required. In the case of using output resistance, output resistance is placed close to the receiver. Additionally, it is recommended that each space between differential output lines such as DMO1P/DMO1N, DMO2P/DMO2N, or DCKP/DCKN is identical, the length of all differential output lines is same, and output line length between the transmitter and the receiver is minimum.

2-1.2 Output Lane

Two or Four data output Lanes are applied from MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) Version 1.00.

2-1.2.1 2Lane Output

Outputs of data and clock come from CSI-2 output pins (DMO1P/DMO1N, DMO2P/DMO2N, DCKP/DCKN). A pair of DMO1P/DMO1N is called Lane1 data and a pair of DMO2P/DMO2N is called Lane2 data. Also, clock signals come from CSI-2 output pins, DCKP/DCKN. Maximum output data rate is 750 Mbps/lane.
For 2Lane output, following register settings are required (1lane output is not supported).

Index	Bit	Register Name	RW	Comment	Default	Desired
0x0309	[3:0]	OPPXCK_DIV	RW	op_pix_clk_div	0x05	0x0A
0x3364	[1:0]	CSI_LANE_MODE	RW	CSI_lane_mode 0: 4 lane, 2: 2lane,	0x00	0x02

3. Control Registers

The IMX179 can use the 2-wire serial communication method for sensor control. These specifications are described for sensor control using the 2-wire serial communication as follows.

3-1 2-wire Serial Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Instance (CCI). CCI is an I^2C fast-mode compatible interface, and the data transfer protocol is I^2C standard.
This 2-wire serial communication circuit can be used to access the control-registers and status-registers of IMX179.

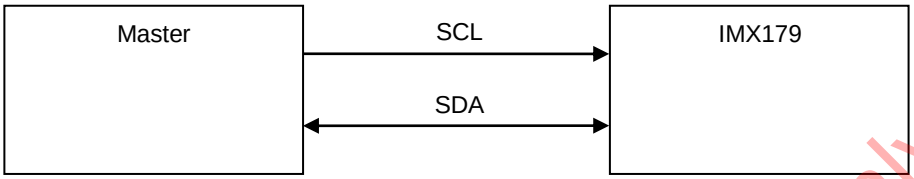


Fig. 5 2-wire Serial Communication

Table. 3 Description of 2-wire Serial Communication Pins

Symbol	Description
SDA	Serial data communication
SCL	Serial clock input

3-1.1 Communication protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

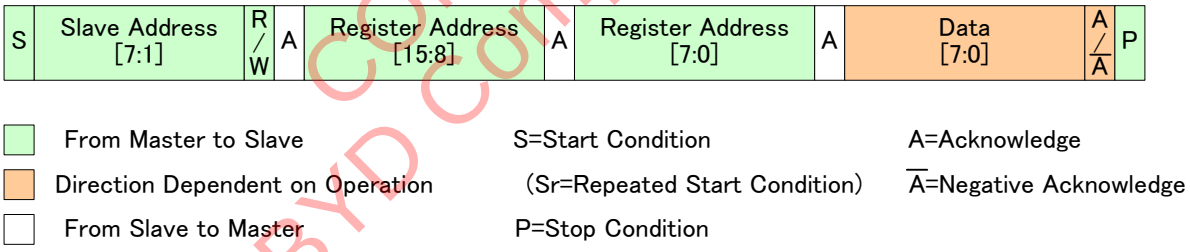


Fig. 6 2-wire Serial Communication protocol

Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred,
A (Acknowledge)/Ā (NegativeAcknowledge) is transferred. Data (SDA) is transferred at the clock (SCL) cycle.
SDA can change only while SCL is Low, so the SDA value must be held while SCL is High.
The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.

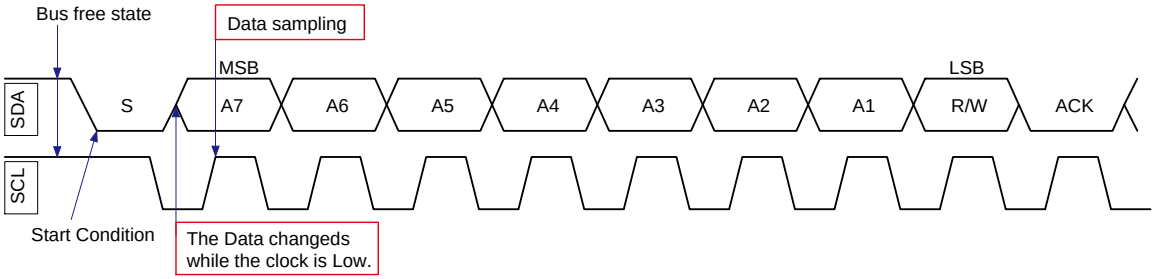


Fig. 7 Start Condition

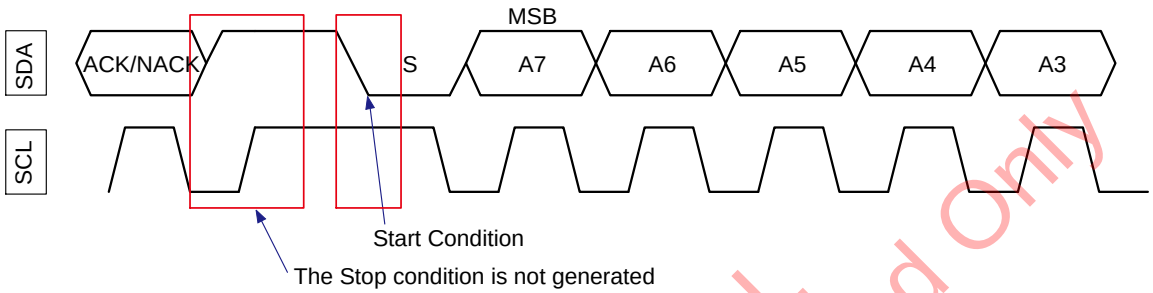


Fig. 8 Repeated Start Condition

The Stop condition is defined by SDA changing from Low to High while SCL is High.

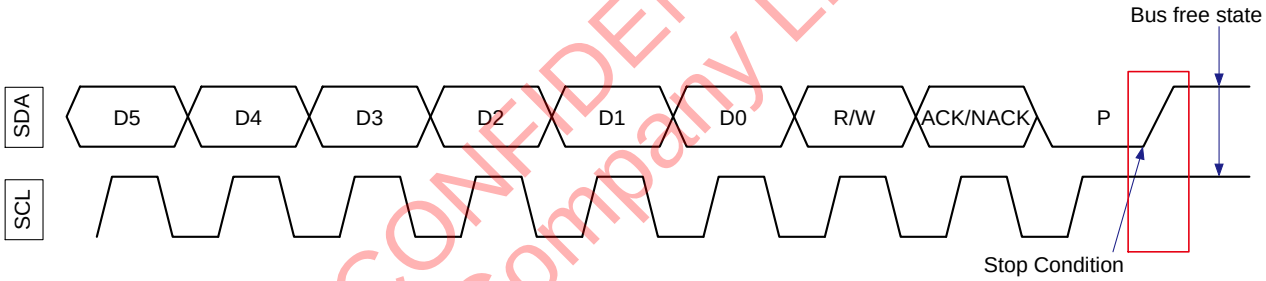


Fig. 9 Stop Condition

The slave address is as follows.

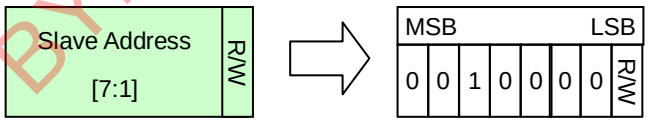


Fig. 10 Slave Address (Default)

The R/W bit indicates the data transfer direction.

Table. 4 R/W Bit

R/W bit	Transfer direction
0	Write (Master →Sensor)
1	Read (Sensor → Master)

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and releases (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop condition and end the communication.

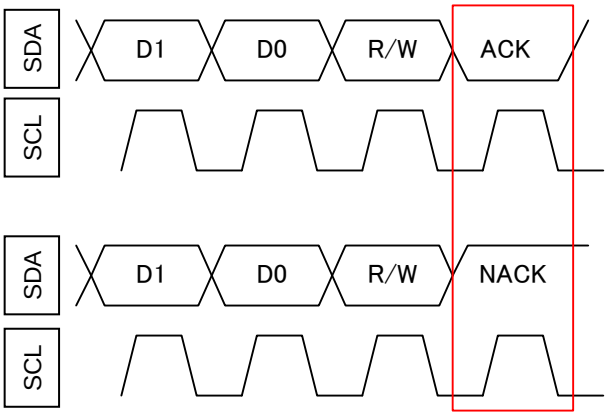


Fig. 11 Acknowledge and Negative Acknowledge

The registers have a 16-bit address space, and are assigned as follows.

Table. 5 2-wire Serial Communication Address Space

Address area	Description
0x0000 - 0x0FFF	Configuration register
0x1000 - 0x1FFF	Parameter limit register Read Only and Static register
0x2000 - 0x2FFF	Image statistics register
0x3000 - 0x3FFF	Manufacture specific register

3-1.2 2-wire serial communication read/write operation supported by the IMX179

The IMX179 supports the following four read operations and two write operations that conform to the SMIA standard

Table. 6 Operations Supported by 2-wire Serial Communication

1	CCI Single read from random location (Single read from an optional address)
2	CCI Single read from current location (Single read from the held address)
3	CCI sequential read starting from random location (Sequential read starting from an optional address)
4	CCI sequential read starting from current location (Sequential read starting from the held address)
5	CCI single write to random location (Single write to an optional address)
6	CCI sequential write starting from random location (Sequential write starting from an optional address)

3-1.2.1 CCI single read from random location

The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start condition is generated without generating the Stop condition, so it becomes the Repeated Start condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop condition to end the communication.

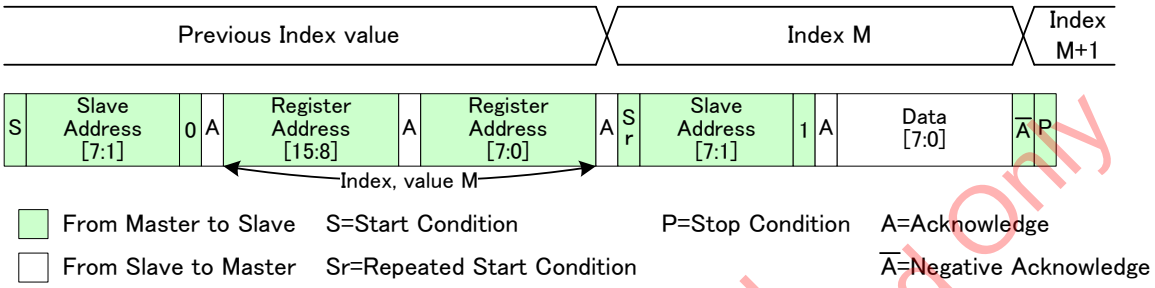


Fig. 12 CCI single read from random location

3-1.2.2 CCI single read from current location

After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.

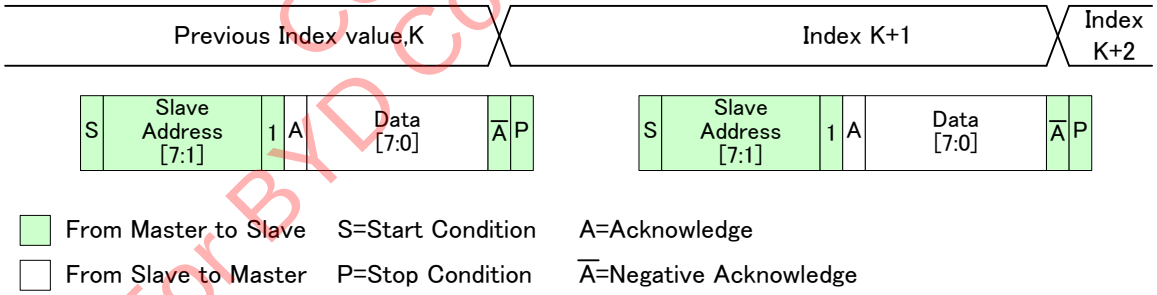


Fig. 13 CCI single read from current location

3-1.2.3 CCI sequential read starting from random location

In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop condition to end the communication.

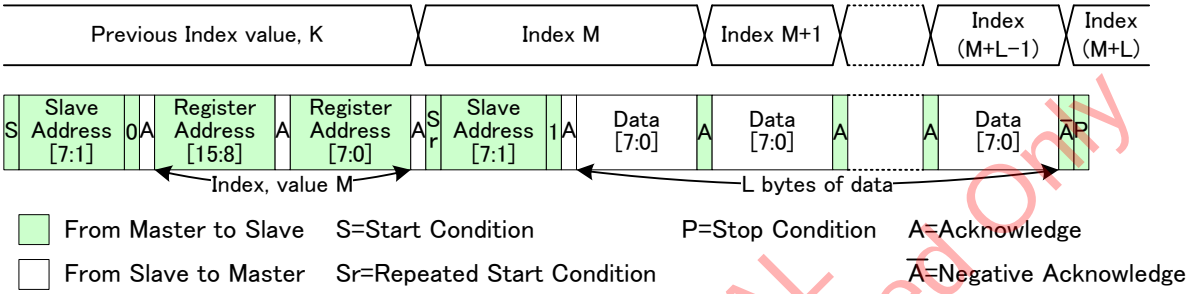


Fig. 14 CCI sequential read starting from random location

3-1.2.4 CCI sequential read starting from current location

When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop condition to end the communication.

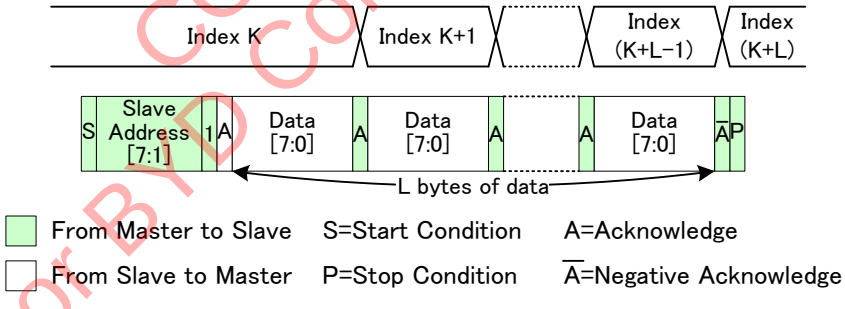


Fig. 15 CCI sequential read starting from current location

3-1.2.5 CCI single write to random location

The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop condition to end the communication.

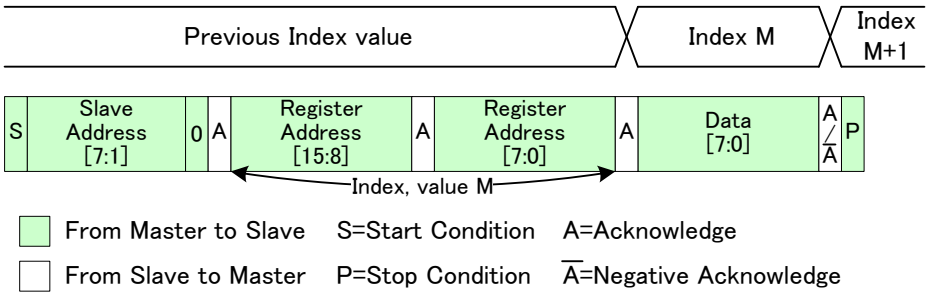


Fig. 16 CCI single write to random location

3-1.2.6 CCI sequential write starting from random location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop condition to end the communication.

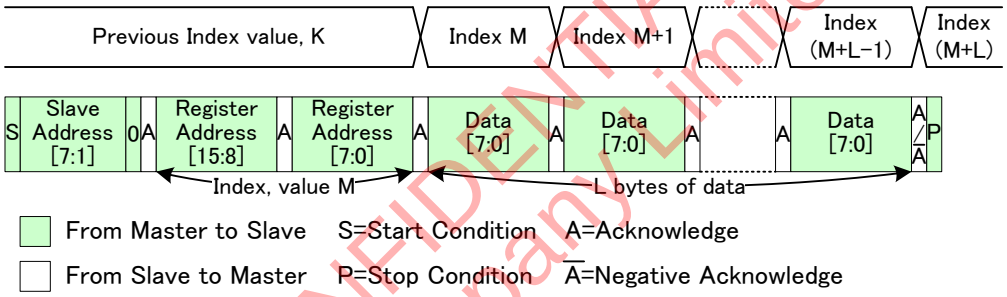


Fig. 17 CCI sequential write starting from random location

3-1.3 2-wire serial communication block characteristics

The block operation specifications for 2-wire serial communication are show below.

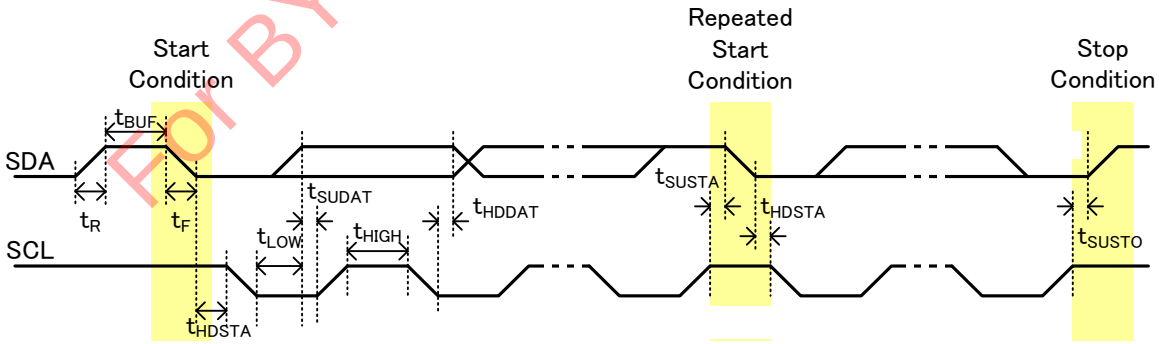


Fig. 18 2-wire Serial Communication Specifications

Table. 7 2-wire Serial Communication Operation Specifications

Item	Symbol	Conditions	Min.	Max.	Unit
Low level input voltage	V_{IL}		-0.5	0.3VDIG	V
High level input voltage	V_{IH}		0.7VDIG	VDIG + 0.5	V
Low level output voltage	V_{OL}	VDIG < 2 V,Sink 2 mA		0.25VDIG	V
High level output voltage	V_{OH}	VDIG < 2 V,Sink 2 mA	0.75VDIG		V
Output fall time	t_{of}	Load 10 pF - 400 pF,0.7VDIG → 0.3VDIG		250	ns
Input current	I_I	0.1VDIG -0.9VDIG	-10	10	µA
SDA I/O capacitance	$C_{I/O}$			8	pF
SCL Input capacitance	C_I			6	pF

Table. 8 2-wire Serial Communication AC Timing

Item	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Rise time (SDA and SCL)	t_R	—	300	ns
Fall time (SDA and SCL)	t_F	—	300	ns
Hold time (start condition)	t_{HDSTA}	0.6	—	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.6	—	µs
Setup time (stop condition)	t_{SUSTO}	0.6	—	µs
Data setup time	t_{SUDAT}	100	—	ns
Data hold time	t_{HDDAT}	0	0.9	µs
Bus free time between Stop and Start condition	t_{BUF}	1.3		µs
Low period of the SCL clock	t_{LOW}	1.3		µs
High period of the SCL clock	t_{HIGH}	0.6		µs

3-1.4 2-wire serial communication register map

3-1.4.1 Description of 2-wire communication register map

In 2-wire serial communication, there is a 16-bit address space as follows. In IMX179, there are partially unreadable registers, which is described in Register map. If reading unreadable registers, the value to be read is 00h.

Table. 9 2-wire Serial Communication Register Map Address Areas

Address Area	Description
0x0000 - 0x0fff	Configuration register
0x1000 - 0x1fff	Parameter limit register Read Only and Static resister
0x2000 - 0x2fff	Reserved for Image statistics register
0x3000 - 0x5fff	Manufacture specific register

3-1.5 Register Re-timing (Grouped Parameter Hold)

Register re-timing sequence is the followings;
"Registers defined as group parameter hold are re-timed in next frame start."

3-2 2-wire Serial Communication Register Map (Configuration register, Parameter limit register)

3-2.1 Configuration Registers – [0x0000-0x00C7]

3-2.1.1 Status Registers – [0x0000-0x0016] (Read Only Dynamic Registers)

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0000	[7:0]	Fabrication	RO	fab_rev_id [7:4]: FAB ID [3:0]: Revision ID of the Type		XX	
0001	[7:0]	Lot_ID[39:32]	RO	Lot_ID of the sensor Copied from NVM 0x3EE to 0x3F2 Type ID is implemented at 0x0002[3:0] – 0x0003[7:0]		XX	○
0002	[7:0]	Lot_ID[31:24]	RO			X1	○
0003	[7:0]	Lot_ID[23:16]	RO			79	○
0004	[7:0]	Lot_ID[15:8]	RO			XX	○
0005	[7:0]	Lot_ID[7:0]	RO			XX	○
0006	—	—	—			00	
0007	[7:0]	Wafer_Num	RO	Wafer Number of the Sensor in the Lot. Value 0x01-0x19 is available.		XX	○
0008	[7:0]	Chip_Number[15:8]	RO	Chip ID in the wafer		XX	○
0009	[7:0]	Chip_Number[7:0]	RO			XX	○
000A	[7:0]	Module_Date[15:8]	RO	Module Production Date and NVM version [15:13]: NVM version [12:9]: Production Year (least two digits) [8:3]: work week (1 to 53) [2:0]: Day in the week. 1 (Monday) to 7 (Sunday)		00	○
000B	[7:0]	Module_Date[7:0]	RO			00	○
000C	—	—	—			00	○
000D	[7:0]	Module_Serial_ID[23:16]	RO	Serial ID of the Module		00	○
000E	[7:0]	Module_Serial_ID[15:8]	RO			00	○
000F	[7:0]	Module_Serial_ID[7:0]	RO			00	○
0010	[7:0]	Module_Parts_ID[15:8]	RO			00	
0011	[7:0]	Module_Parts_ID[7:0]	RO			00	
0012	[7:0]	FRM_CNT[7:0]	RO			FF	○
0013	[7:0]	PX_ORDER	RO			01	○
0014	[1:0]	DT_PEDESTAL[9:8]	RO			40	○
0015	[7:0]	DT_PEDESTAL[7:0]					○
0016	[7:0]	PIXEL_DEPTH	RO			0A	○

3-2.1.2 Frame Format Description – [0x0040-0x0047]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0040	[7:0]	FRM_FMT_TYPE[7:0]	RO	frame_format_model_type		01	○
0x0041	[7:0]	FRM_FMT_SUBTYPE[7:0]	RO	frame_format_model_subtype		12	○
0x0042	[7:0]	FRM_FMT_DESC0[15:8]	RO-D	frame_format_descriptor_0		5C	○
0x0043	[7:0]	FRM_FMT_DESC0[7:0]				D0	○
0x0044	[7:0]	FRM_FMT_DESC1[15:8]	RO	frame_format_descriptor_1		10	○
0x0045	[7:0]	FRM_FMT_DESC1[7:0]				02	○
0x0046	[7:0]	FRM_FMT_DESC2[15:8]	RO-D	frame_format_descriptor_2		59	○
0x0047	[7:0]	FRM_FMT_DESC2[7:0]				A0	○

3-2.1.3 Analogue Gain Description Registers – [0x0080-0x0093]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0080	—					00	○
0x0081	[0]	analogue_gain_capability	RO	Analogue Gain Description Registers		00	○
0x0082	—	Reserved	RO	Reserved		00	
0x0083	—		RO			00	
0x0084	—					00	○
0x0085	[7:0]	analogue_gain_code_min	RO	Analogue Gain Description Registers		00	○
0x0086	[7:0]	analogue_gain_code_max	RO	Analogue Gain Description Registers		00	○
0x0087	[7:0]		RO			E0	○
0x0088	[7:0]	analogue_gain_code_step	RO	Analogue Gain Description Registers		00	○
0x0089	[7:0]		RO			01	○
0x008A	[7:0]	analogue_gain_type	RO	Analogue Gain Description Registers		00	○
0x008B	[7:0]		RO			00	○
0x008C	[7:0]	analogue_gain_m0	RO	Analogue Gain Description Registers		00	○
0x008D	[7:0]		RO			00	○
0x008E	[7:0]	analogue_gain_c0	RO	Analogue Gain Description Registers		01	○
0x008F	[7:0]		RO			00	○
0x0090	[7:0]	analogue_gain_m1	RO	Analogue Gain Description Registers		FF	○
0x0091	[7:0]		RO			FF	○
0x0092	[7:0]	analogue_gain_c1	RO	Analogue Gain Description Registers		01	○
0x0093	[7:0]		RO			00	○

3-2.1.4 Data Format Description – [0x00C0-0x00C7]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x00C0	[7:0]	DT_FMT_TYPE[7:0]	RO	data_format_model_type		01	○
0x00C1	[7:0]	DT_FMT_SUBTYPE[7:0]	RO	data_format_model_subtype		03	○
0x00C2	[7:0]	DT_FMT_DESC0[15:8]	RO	data_format_descriptor_0		08	○
0x00C3	[7:0]	DT_FMT_DESC0[7:0]				08	○
0x00C4	[7:0]	DT_FMT_DESC1[15:8]	RO	data_format_descriptor_1		0A	○
0x00C5	[7:0]	DT_FMT_DESC1[7:0]				08	○
0x00C6	[7:0]	DT_FMT_DESC2[15:8]	RO	data_format_descriptor_2		0A	○
0x00C7	[7:0]	DT_FMT_DESC2[7:0]				0A	○

3-2.2 Set-up Registers – [0x0100-0x0FFF]

3-2.2.1 General Set-up Registers – [0x0100-0x0105]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0100		mode_select	RW	Mode Select: 0: SW standby, 1: Streaming		0	○
0x0101	[1:0]	IMG_ORIENTATION	RW	image_orientation bit[0]: horizontal direction, bit[1]: vertical direction	GPH	0	○
0x0102		Reserved					
0x0103	[0]	SW_RESET	RW	software_reset		0	○
0x0104	[0]	GRP_PARAM_HOLD	RW	grouped_parameter_hold		0	○
0x0105	[0]	MASK_CORR_FRM	RO	mask_corrupted_frames		1	○

3-2.2.2 Output Set-up Registers – [0x0200-0x0215]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0200	[7:0]	FINE_INTEG_TIME[15:8]	RO	fine_integration_time		01	○
0x0201	[7:0]	FINE_INTEG_TIME[7:0]	RO			E8	○
0x0202	[7:0]	COARSE_INTEG_TIME[15:8]	RW	coarse_integration_time	GPH	03	○
0x0203	[7:0]	COARSE_INTEG_TIME[7:0]	RW		GPH	E8	○
0x0205	[7:0]	ANA_GAIN_GLOBAL	RW	analogue_gain_code_global	GPH	00	○
0x020E	[3:0]	DIG_GAIN_GR[11:8]	RW	digital_gain_greenR	GPH	01	○
0x020F	[7:0]	DIG_GAIN_GR[7:0]	RW		GPH	00	○
0x0210	[3:0]	DIG_GAIN_R[11:8]	RW	digital_gain_red	GPH	01	○
0x0211	[7:0]	DIG_GAIN_R[7:0]	RW		GPH	00	○
0x0212	[3:0]	DIG_GAIN_B[11:8]	RW	digital_gain_blue	GPH	01	○
0x0213	[7:0]	DIG_GAIN_B[7:0]	RW		GPH	00	○
0x0214	[3:0]	DIG_GAIN_GB[11:8]	RW	digital_gain_greenB	GPH	01	○
0x0215	[7:0]	DIG_GAIN_GB[7:0]	RW		GPH	00	○

3-2.2.3 Clock Set-up Registers – [0x0300-0x030D]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0300	—	—	RW				○
0x0301	[3:0]	VTPXCK_DIV	RW	vt_pix_clk_div		A	○
0x0302	—	—	RW				○
0x0303	[1:0]	VTSYCK_DIV	RW	vt_sys_clk_div		01	○
0x0305	[3:0]	PREPLLCK_ DIV	RW	pre_pll_clk_ div		B	○
0x0308	—	—	RW				○
0x0309	[3:0]	OPPXCK_DIV	RW	op_pix_clk_div		5	○
0x030A	—	—	RW				
0x030B	[1:0]	OPSYCK_DIV	RW	op_sys_clk_div		1	○
0x030C	[2:0]	PLL_MPY[10:8]	RW	pll_multiplier		2	○
0x030D	[7:0]	PLL_MPY[7:0]	RW			BC	○

3-2.2.4 Frame Timing Registers – [0x0340-0x0343]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0340	[7:0]	FRM_LENGTH[15:8]	RW	frame_length_lines	GPH	0A	○
0x0341	[7:0]	FRM_LENGTH[7:0]	RW		GPH	20	○
0x0342	[7:0]	LINE_LENGTH[15:8]	RW	line_length_pck	GPH	0E	○
0x0343	[7:0]	LINE_LENGTH[7:0]	RW		GPH	10	○

3-2.2.5 Image Size Registers – [0x0344-0x034F]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0344	[7:0]	X_ADD_STA[11:8]	RW	x_addr_start	GPH	00	○
0x0345	[7:0]	X_ADD_STA[7:0]	RW		GPH	00	○
0x0346	[7:0]	Y_ADD_STA[11:8]	RW	y_addr_start	GPH	00	○
0x0347	[7:0]	Y_ADD_STA[7:0]	RW		GPH	00	○
0x0348	[7:0]	X_ADD_END[11:8]	RW	x_addr_end	GPH	0C	○
0x0349	[7:0]	X_ADD_END[7:0]	RW		GPH	CF	○
0x034A	[7:0]	Y_ADD_END[11:8]	RW	y_addr_end	GPH	09	○
0x034B	[7:0]	Y_ADD_END[7:0]	RW		GPH	9F	○
0x034C	[7:0]	X_OUT_SIZE[11:8]	RW	x_output_size	GPH	0C	○
0x034D	[7:0]	X_OUT_SIZE[7:0]	RW		GPH	D0	○
0x034E	[7:0]	Y_OUT_SIZE[11:8]	RW	y_output_size	GPH	09	○
0x034F	[7:0]	Y_OUT_SIZE[7:0]	RW		GPH	A0	○

3-2-2-6 Sub-Sampling Registers – [0x0380-0x0387]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0380	—	—			—	00	○
0x0381	[2:0]	X_EVN_INC	RW	x_even_inc	GPH	01	○
0x0382	—	—			—	00	○
0x0383	[2:0]	X_ODD_INC	RW	x_odd_inc	GPH	01	○
0x0384	—	—			—	00	○
0x0385	[2:0]	Y_EVN_INC	RW	y_even_inc	GPH	01	○
0x0386	—	—			—	00	○
0x0387	[2:0]	Y_ODD_INC	RW	y_odd_inc	GPH	01	○

3-2-2-7 Binning Registers – [0x0390]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0390	[1:0]	BINNING_MODE	RW	Defines binning mode. 0:no-binning 1:2x2-binning 2:4x4-binning	GPH	00	○

3-2-2-8 Image Scaling Registers – [0x0400-0x0407]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0400	—	—	—		—	00	○
0x0401	[1:0]	SCALE_MODE	RW	Scaling_mode	GPH	00	○
0x0402	—	—	—		—	00	○
0x0403	[1:0]	—	—		—	00	○
0x0404	[0]	SCALE_M[8]	RW	scale_m	GPH	00	○
0x0405	[7:0]	SCALE_M[7:0]	RW		GPH	10	○
0x0406	—	—	—		—	00	○
0x0407	[4:0]	SCALE_N	RO	scale_n	GPH	10	○

3-2-2-9 Image Compression Registers – [0x0501]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0501	[0]	COMP_MODE	RW	compression_mode	GPH	01	○

3-2.2.10 Test Pattern Registers – [0x0600-0x0611]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0600	[0]	test_pattern_mode	RW			0	○
0x0601	[7:0]					00	
0x0602	[7:0]	TD_R[9:8]	RW	test_data_red		00	○
0x0603	[7:0]	TD_R[7:0]	RW			00	○
0x0604	[7:0]	TD_GR[9:8]	RW	test_data_greenR		00	○
0x0605	[7:0]	TD_GR[7:0]	RW			00	○
0x0606	[7:0]	TD_B[9:8]	RW	test_data_blue		00	○
0x0607	[7:0]	TD_B[7:0]	RW			00	○
0x0608	[7:0]	TD_GB[9:8]	RW	test_data_greenB		00	○
0x0609	[7:0]	TD_GB[7:0]	RW			00	○
0x060A	[7:0]	H_CUR_WIDTH[15:8]	RW	horizontal_cursor_width		00	○
0x060B	[7:0]	H_CUR_WIDTH[7:0]	RW			00	○
0x060C	[7:0]	H_CUR_POS[15:8]	RW	horizontal_cursor_position		00	○
0x060D	[7:0]	H_CUR_POS[7:0]	RW			00	○
0x060E	[7:0]	V_CUR_WIDTH[15:8]	RW	vertical_cursor_width		00	○
0x060F	[7:0]	V_CUR_WIDTH[7:0]	RW			00	○
0x0610	[7:0]	V_CUR_POS[15:8]	RW	vertical_cursor_position		00	○
0x0611	[7:0]	V_CUR_POS[7:0]	RW			00	○

3-3 Parameter Limit Registers - [0x1000-0x1FFF] (Read Only and Static)

3-3.1 Integration Time and Gain Parameter Limit Registers – [0x1000-0x1301]

3-3.1.1 Integration Time Parameter Limit Registers – [0x1000-0x1007]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x1000	—	integration_time_capability	RO				
0x1001	[0]			0 – coarse integration but NO fine integration		0	
0x1002	—	Reserved	RO				
0x1003	—						
0x1004	[7:0]	coarse_integration_time_min	RO	Lines		00	
0x1005	[7:0]			Format: 16-bits unsigned integer		01	
0x1006	[7:0]	coarse_integration_time_max_margin	RO	(Current frame length – current max coarse exp)		00	
0x1007	[7:0]			Format: 16-bits unsigned integer		04	

3-3.1.2 Digital Gain Parameter Limit Registers – [0x1080-0x1089]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x1080	—		RO				
0x1081	[0]	digital_gain_capability		1 – per channel digital gain		01	
0x1082	—	Reserved	RO			00	
0x1083	—					00	
0x1084	[7:0]	digital_gain_min	RO	Minimum recommended digital gain value		01	
0x1085	[7:0]			Format: 16-bit unsigned 8.8 fixed point number		00	
0x1086	[7:0]	digital_gain_max	RO	Maximum recommended digital gain value		0F	
0x1087	[7:0]			Format: 16-bit unsigned 8.8 fixed point number		FF	
0x1088	[7:0]	digital_gain_step_size	RO	Digital gain step size		00	
0x1089	[7:0]			Format: 16-bit unsigned 8.8 fixed point number		01	

3-3.1.3 Pre-PLL and PLL Clock Set-up Capability Registers – [0x1100-0x111F]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x1100	[7:0]	min_ext_clk_freq_mhz	RO	Minimum external clock frequency		40	
0x1101	[7:0]			Format: IEEE 32-bit float		C0	
0x1102	[7:0]			Units: MHz		00	
0x1103	[7:0]			6 MHz (= min_ext_clk_freq_mhz)		00	
0x1104	[7:0]	max_ext_clk_freq_mhz	RO	Maximum external clock frequency		41	
0x1105	[7:0]			Format: IEEE 32-bit float Units: MHz		D8	
0x1106	[7:0]			27 MHz (= max_ext_clk_freq_mhz)		00	
0x1107	[7:0]					00	
0x1108	[7:0]	min_pre_pll_clk_div	RO	Minimum Pre PLL divider value		00	
0x1109	[7:0]			Format: 16-bit unsigned integer		01	
0x110A	[7:0]	max_pre_pll_clk_div	RO	Maximum Pre PLL divider value		00	
0x110B	[7:0]			Format: 16-bit unsigned integer		0D	
0x110C	[7:0]	min_pll_ip_freq_mhz	RO	Minimum PLL input clock frequency		3F	
0x110D	[7:0]			Format: IEEE 32-bit float Units: MHz		80	
0x110E	[7:0]			1 MHz		00	
0x110F	[7:0]					00	
0x1110	[7:0]	max_pll_ip_freq_mhz	RO	Maximum PLL input clock frequency		41	
0x1111	[7:0]			Format: IEEE 32-bit float Units: MHz		D8	
0x1112	[7:0]			27 MHz (= max_ext_clk_freq_mhz)		00	
0x1113	[7:0]					00	
0x1114	[7:0]	min_pll_multiplier	RO	Minimum PLL multiplier		00	
0x1115	[7:0]			Format: 16-bit unsigned integer		08	
0x1116	[7:0]	max_pll_multiplier	RO	Maximum PLL Multiplier		07	
0x1117	[7:0]			Format: 16-bit unsigned integer		FF	
0x1118	[7:0]	min_pll_op_freq_mhz	RO	Minimum PLL output clock		43	
0x1119	[7:0]			frequency Format: IEEE 32-bit float		A9	
0x111A	[7:0]			Units: MHz		00	
0x111B	[7:0]			338 MHz		00	
0x111C	[7:0]	max_pll_op_freq_mhz	RO	Maximum PLL output clock frequency		44	
0x111D	[7:0]			Format: IEEE 32-bit float		80	
0x111E	[7:0]			Units: MHz		20	
0x111F	[7:0]			1025 MHz		00	

3-3.1.4 Read Domain Clock Set-up Capability Registers – [0x1120-0x1137]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x1120	[7:0]	min_vt_sys_clk_div	RO	Minimum video timing system clock divider value		00	
0x1121	[7:0]			Format: 16-bit unsigned integer		01	
0x1122	[7:0]	max_vt_sys_clk_div	RO	Maximum video timing system clock divider value		00	
0x1123	[7:0]			Format: 16-bit unsigned integer		02	
0x1124	[7:0]	min_vt_sys_clk_freq_mhz	RO	Minimum video timing system clock frequency		43	
0x1125	[7:0]			Format: IEEE 32-bit float Units: MHz		29	
0x1126	[7:0]			169 MHz		00	
0x1127	[7:0]					00	
0x1128	[7:0]	max_vt_sys_clk_freq_mhz	RO	Maximum video timing system clock frequency		44	
0x1129	[7:0]			Format: IEEE 32-bit float Units: MHz		80	
0x112A	[7:0]			1025 MHz		20	
0x112B	[7:0]					00	
0x112C	[7:0]	min_vt_pix_clk_freq_mhz	RO	Minimum video timing pixel clock frequency		41	
0x112D	[7:0]			Format: IEEE 32-bit float Units: MHz		87	
0x112E	[7:0]			16.9 MHz		33	
0x112F	[7:0]					33	
0x1130	[7:0]	max_vt_pix_clk_freq_mhz	RO	Maximum video timing pixel clock frequency		42	
0x1131	[7:0]			Format: IEEE 32-bit float Units: MHz		D4	
0x1132	[7:0]			101 MHz		00	
0x1133	[7:0]					00	
0x1134	[7:0]	min_vt_pix_clk_div	RO	Minimum video timing pixel clock divider value		00	
0x1135	[7:0]			Format: 16-bit unsigned integer		04	
0x1136	[7:0]	max_vt_pix_clk_div	RO	Maximum video timing pixel clock divider value		00	
0x1137	[7:0]			Format: 16-bit unsigned integer		0A	

3-3.1.5 Frame Timing Parameter Limit Registers – [0x1140-0x1149]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x1140	[7:0]	min_frame_length_lines	RO	Minimum Frame Length allowed. Value both sensor dependent		00	
0x1141	[7:0]			Format: 16-bit unsigned integer Units: Lines		AC	
0x1142	[7:0]	max_frame_length_lines	RO	Maximum possible number of lines per Frame. Value sensor dependent		FF	
0x1143	[7:0]			Format: 16-bit unsigned integer Units: Lines		FF	
0x1144	[7:0]	min_line_length_pck	RO	Minimum Line Length allowed. Value sensor dependent		0D	
0x1145	[7:0]			Format: 16-bit unsigned integer Units: Pixel Clock		48	
0x1146	[7:0]	max_line_length_pck	RO	Maximum possible number of pixel clocks per line. Value sensor dependent		7F	
0x1147	[7:0]			Format: 16-bit unsigned integer Units: Pixel Clock		F0	
0x1148	[7:0]	min_line_blanking_pck	RO	Minimum line blanking time in pixel clocks		00	
0x1149	[7:0]			Format: 16-bit unsigned integer Units: Pixel Clock		78	

3-3.1.6 Output Clock Set-up Capability Registers – [0x1160-0x1177]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x1160	[7:0]	min_op_sys_clk_div	RO	Minimum output system clock divider value		00	
0x1161	[7:0]			Format: 16-bit unsigned integer		01	
0x1162	[7:0]	max_op_sys_clk_div	RO	Maximum output system clock divider value		00	
0x1163	[7:0]			Format: 16-bit unsigned integer		02	
0x1164	[7:0]	min_op_sys_clk_freq_mhz	RO	Minimum output system clock frequency		43	
0x1165	[7:0]			Format: IEEE 32-bit float		29	
0x1166	[7:0]			Units: MHz		00	
0x1167	[7:0]			169 MHz		00	
0x1168	[7:0]	max_op_sys_clk_freq_mhz	RO	Maximum output system clock frequency		44	
0x1169	[7:0]			Format: IEEE 32-bit float Units: MHz		80	
0x116A	[7:0]			1025 MHz		20	
0x116B	[7:0]					00	
0x116C	[7:0]	min_op_pix_clk_div	RO	Minimum output pixel clock divider value		00	
0x116D	[7:0]			Format: 16-bit unsigned integer		04	

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x116E	[7:0]	max_op_pix_clk_div	RO	Maximum output pixel clock divider value		00	
0x116F	[7:0]			Format: 16-bit unsigned integer		0A	
0x1170	[7:0]	min_op_pix_clk_freq_mhz	RO	Minimum output pixel clock frequency		41	
0x1171	[7:0]			Format: IEEE 32-bit float Units: MHz		87	
0x1172	[7:0]			16.9 MHz		33	
0x1173	[7:0]					33	
0x1174	[7:0]	max_op_pix_clk_freq_mhz	RO	Maximum output pixel clock frequency		42	
0x1175	[7:0]			Format: IEEE 32-bit float Units: MHz		F0	
0x1176	[7:0]			101 MHz		00	
0x1177	[7:0]					00	

3-3.1.7 Image Size Parameter Limit Registers – [0x1180-0x1187]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x1180	[7:0]	x_addr_min	RO	Minimum X-address of the addressable pixel array Format: 16-bit unsigned integer		00	
0x1181	[7:0]			Value: Always 0		00	
0x1182	[7:0]	y_addr_min	RO	Minimum Y-address of the addressable pixel array Format: 16-bit unsigned integer		00	
0x1183	[7:0]			Value: Always 0		00	
0x1184	[7:0]	x_addr_max	RO	Maximum X-address of the addressable pixel array Format: 16-bit unsigned integer		0C	
0x1185	[7:0]					CF	
0x1186	[7:0]	y_addr_max	RO	Maximum Y-address of the addressable pixel array Format: 16-bit unsigned integer		09	
0x1187	[7:0]					9F	

3-3.1.8 Sub-Sampling Parameter Limit Registers – [0x11C0-0x11C7]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x11C0	[7:0]	min_even_inc	RO	Minimum Increment for even pixels		00	
0x11C1	[7:0]			Format: 16-bit unsigned integer (static)		01	
0x11C2	[7:0]	max_even_inc	RO	Maximum increment for even pixels		00	
0x11C3	[7:0]			Format: 16-bit unsigned integer (static)		01	
0x11C4	[7:0]	min_odd_inc	RO	Minimum Increment for odd pixels		00	
0x11C5	[7:0]			Format: 16-bit unsigned integer (static)		01	
0x11C6	[7:0]	max_odd_inc	RO	Maximum Increment for odd pixels		00	
0x11C7	[7:0]			Format: 16-bit unsigned integer (static)		03	

3-3.1.9 Image Scaling Parameter Limit Registers – [0x1200-0x120B]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x1200	—						
0x1201	[1:0]	scaling_capability	RO	0 – None; 1 – H dir 2 – Full (H & V), Format: 16-bit unsigned integer		02	
0x1202	—	Reserved	RO				
0x1203	—						
0x1204	—					00	
0x1205	[4:0]	scaler_m_min	RO	Down scale factor: Minimum M value Value is always 16 Format: 16-bit unsigned integer		10	
0x1206	[0]	scaler_m_max	RO	Down scale factor: Maximum M value		01	
0x1207	[7:0]			Format: 16-bit unsigned integer		00	
0x1208	—						
0x1209	[4:0]	scaler_n_min	RO	Down scale factor: Min. N value Value = 16, Format: 16-bit unsigned integer		10	
0x120A	—						
0x120B	[4:0]	scaler_n_max	RO	Down scale factor: Min. N value Value = 16, Format: 16-bit unsigned integer		10	

3-3.1.10 Image Compression Capability Registers – [0x1300-0x1301]

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x1300	—						
0x1301	[0]	compression_capability	RO	0 – No Compression; 1 – DPCM/PCM Compression		01	

3-4 Manufacturer Specific Registers - [0x3000-0x3FFF]

3-4.1 [0x3000-0x30FF]

Index (HEX)	Bit	Register Name	RW	Comment	Re-Timed	Default (HEX)
3344	[7:0]	RGTHSEXIT	RW	Timer value of Ths-exit		0
3345	[7:0]	RGTCLKPRE	RW	Timer value of Tclk-pre		0
3346	[3:0]	RGTLPXESC	RW	Timer value of Tlpx (TxClkEsc) (valid only during SW-standby)		2
3360	[2:0]	CSI2_CHID	RW	CSI_channel_identifier	GPH	00
3362	[7:0]	CSI_DT_FMT[15:8]	RW	CSI_data_format		0A
3363	[7:0]	CSI_DT_FMT[7:0]	RW			0A
3364	[1:0]	CSI_LANE_MODE	RW	CSI_lane_mode 0: 4 lane, 2: 2lane		00
3368	[7:0]	INCK_FREQ[15:8]	RW	input_clk_frequency_mhz		0B
3369	[7:0]	INCK_FREQ[7:0]	RW			6E

Index (HEX)	Bit	Register Name	RW	Comment	Re-Timed	Default (HEX)
3370	[7:0]	TCLK_POST	RW	tclk_post		0
3371	[7:0]	THS_PREPARE	RW	ths_prepare		0
3372	[7:0]	THS_ZERO_Min.	RW	ths_zero_min		0
3373	[7:0]	THS_TRAIL	RW	ths_trail		0
3374	[7:0]	TCLK_TRAIL_Min.	RW	tclk_trail_min		0
3375	[7:0]	TCLK_PREPARE	RW	tclk_prepare		0
3376	[7:0]	TCLK_ZERO	RW	tclk_zero		0
3377	[7:0]	TLPX	RW	tlpx		0
3378	[7:0]	CSI2_COMP8_DT	RW	visible data type for comp-8 output		30
33C8	[2]	Binning_Cal	RW	0: Average, 1: Sum	GPH	0

3-4.2 [0x3400-0x34FF]

Index (HEX)	Bit	Register Name	RW	Comment	Re-Timed	Default (HEX)
3400	[2:0]	OTPIF_CTRL	RW	OTP I/F control register [0] enable [1]R/W [2]error clear		0
3401	[1:0]	OTPIF_STATUS	RO-D	OTP I/F status; [0] ready [1] error		0
3402	[2:0]	OTPIF_PAGE_SELECT	RW	otpif_page_select		0
3404	[7:0]	OTPIF_DT_0	RW	otpif_data_0		0
3405	[7:0]	OTPIF_DT_1	RW	otpif_data_1		0
3406	[7:0]	OTPIF_DT_2	RW	otpif_data_2		0
3407	[7:0]	OTPIF_DT_3	RW	otpif_data_3		0
3408	[7:0]	OTPIF_DT_4	RW	otpif_data_4		0
3409	[7:0]	OTPIF_DT_5	RW	otpif_data_5		0
340A	[7:0]	OTPIF_DT_6	RW	otpif_data_6		0
340B	[7:0]	OTPIF_DT_7	RW	otpif_data_7		0
340C	[7:0]	OTPIF_DT_8	RW	otpif_data_8		0
340D	[7:0]	OTPIF_DT_9	RW	otpif_data_9		0
340E	[7:0]	OTPIF_DT_10	RW	otpif_data_10		0
340F	[7:0]	OTPIF_DT_11	RW	otpif_data_11		0
3410	[7:0]	OTPIF_DT_12	RW	otpif_data_12		0
3411	[7:0]	OTPIF_DT_13	RW	otpif_data_13		0
3412	[7:0]	OTPIF_DT_14	RW	otpif_data_14		0
3413	[7:0]	OTPIF_DT_15	RW	otpif_data_15		0
3414	[7:0]	OTPIF_DT_16	RW	otpif_data_16		0
3415	[7:0]	OTPIF_DT_17	RW	otpif_data_17		0
3416	[7:0]	OTPIF_DT_18	RW	otpif_data_18		0
3417	[7:0]	OTPIF_DT_19	RW	otpif_data_19		0
3418	[7:0]	OTPIF_DT_20	RW	otpif_data_20		0
3419	[7:0]	OTPIF_DT_21	RW	otpif_data_21		0
341A	[7:0]	OTPIF_DT_22	RW	otpif_data_22		0

Index (HEX)	Bit	Register Name	RW	Comment	Re-Timed	Default (HEX)
341B	[7:0]	OTPIF_DT_23	RW	otpif_data_23		0
341C	[7:0]	OTPIF_DT_24	RW	otpif_data_24		0
341D	[7:0]	OTPIF_DT_25	RW	otpif_data_25		0
341E	[7:0]	OTPIF_DT_26	RW	otpif_data_26		0
341F	[7:0]	OTPIF_DT_27	RW	otpif_data_27		0
3420	[7:0]	OTPIF_DT_28	RW	otpif_data_28		0
3421	[7:0]	OTPIF_DT_29	RW	otpif_data_29		0
3422	[7:0]	OTPIF_DT_30	RW	otpif_data_30		0
3423	[7:0]	OTPIF_DT_31	RW	otpif_data_31		0
3424	[7:0]	OTPIF_DT_32	RW	otpif_data_32		0
3425	[7:0]	OTPIF_DT_33	RW	otpif_data_33		0
3426	[7:0]	OTPIF_DT_34	RW	otpif_data_34		0
3427	[7:0]	OTPIF_DT_35	RW	otpif_data_35		0
3428	[7:0]	OTPIF_DT_36	RW	otpif_data_36		0
3429	[7:0]	OTPIF_DT_37	RW	otpif_data_37		0
342A	[7:0]	OTPIF_DT_38	RW	otpif_data_38		0
342B	[7:0]	OTPIF_DT_39	RW	otpif_data_39		0
342C	[7:0]	OTPIF_DT_40	RW	otpif_data_40		0
342D	[7:0]	OTPIF_DT_41	RW	otpif_data_41		0
342E	[7:0]	OTPIF_DT_42	RW	otpif_data_42		0
342F	[7:0]	OTPIF_DT_43	RW	otpif_data_43		0
3430	[7:0]	OTPIF_DT_44	RW	otpif_data_44		0
3431	[7:0]	OTPIF_DT_45	RW	otpif_data_45		0
3432	[7:0]	OTPIF_DT_46	RW	otpif_data_46		0
3433	[7:0]	OTPIF_DT_47	RW	otpif_data_47		0
3434	[7:0]	OTPIF_DT_48	RW	otpif_data_48		0
3435	[7:0]	OTPIF_DT_49	RW	otpif_data_49		0
3436	[7:0]	OTPIF_DT_50	RW	otpif_data_50		0
3437	[7:0]	OTPIF_DT_51	RW	otpif_data_51		0
3438	[7:0]	OTPIF_DT_52	RW	otpif_data_52		0
3439	[7:0]	OTPIF_DT_53	RW	otpif_data_53		0
343A	[7:0]	OTPIF_DT_54	RW	otpif_data_54		0
343B	[7:0]	OTPIF_DT_55	RW	otpif_data_55		0
343C	[7:0]	OTPIF_DT_56	RW	otpif_data_56		0
343D	[7:0]	OTPIF_DT_57	RW	otpif_data_57		0
343E	[7:0]	OTPIF_DT_58	RW	otpif_data_58		0
343F	[7:0]	OTPIF_DT_59	RW	otpif_data_59		0
3440	[7:0]	OTPIF_DT_60	RW	otpif_data_60		0
3441	[7:0]	OTPIF_DT_61	RW	otpif_data_61		0
3442	[7:0]	OTPIF_DT_62	RW	otpif_data_62		0
3443	[7:0]	OTPIF_DT_63	RW	otpif_data_63		0

3-4.3 [0x4100-0x41FF]

Index (HEX)	Bit	Register Name	RW	Comment	Re-Timed	Default (HEX)
4100	[2]	ZNR_FD_DFCT_SW	RW	0: Static Mode Off 1: Static Mode On	V-Sync	0
4100	[5:3]	ZNR_DIFF_DFCT_SW	RW	[3]: Dynamic Mode-1 [4]: Dynamic Mode-2 [5]: Dynamic Mode-3	V-Sync	1
4102	[4:0]	ZNR_Coefficient1	RW	Parameter Setting1		A
4103	[7:0]	ZNR_Coefficient2	RW	Parameter Setting2		0
4104	[6:0]	ZNR_Coefficient3	RW	Parameter Setting3		32
4105	[6:0]	ZNR_Coefficient4	RW	Parameter Setting4		32
4106	[6:0]	ZNR_Coefficient5	RW	Parameter Setting5		40
4107	[6:0]	ZNR_Coefficient6	RW	Parameter Setting6		40
4108	[1:0]	ZNR_Coefficient7 [9:8]	RW	Parameter Setting7		0
4109	[7:0]	ZNR_Coefficient7 [7:0]	RW			
410A	[1:0]	ZNR_Coefficient8 [9:8]	RW	Parameter Setting8		0
410B	[7:0]	ZNR_Coefficient8 [7:0]	RW			
410C	[1:0]	ZNR_Coefficient9 [9:8]	RW	Parameter Setting9		0
410D	[7:0]	ZNR_Coefficient9 [7:0]	RW			
410E	[1:0]	ZNR_Coefficient10 [9:8]	RW	Parameter Setting10		0
410F	[7:0]	ZNR_Coefficient10 [7:0]	RW			

Note) Write to blank addresses is prohibited.
For “Test register”, setting registers is prohibited.

3-4.4 Startup Sequence in 2-wire Serial Communication Mode

Perform power-on according to the following sequence.

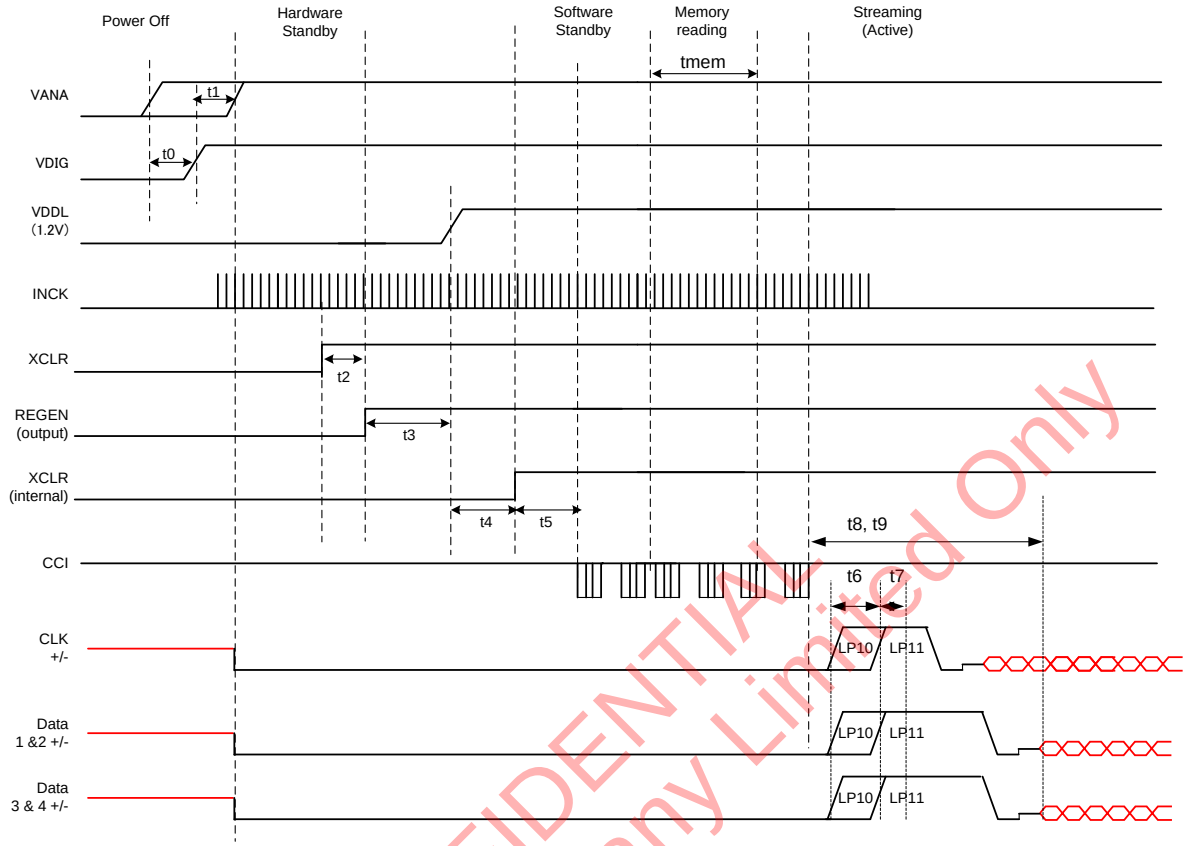


Fig. 19 Power-on Sequence in 2-wire Serial Communication Mode

Table. 10 Operation Specifications 2-wire Serial Communication Mode

Constraint	Label	Min.	Max.	Units	Comment
Sequence free of VANA rising and VDIG rising	t0, t1	VANA and VDIG may rise in any order.		ns	
Time to REGEN Low to High after XCLR Low to High	t2		0.5	µs	
Time to VDDL is supplied to sensor after REGEN high	t3			µs	Depending on Device
Internal XCLR is Low to High after VDDL is supplied	t4	100	600	µs	Waking up time and init settings
Initializing time of silicon	t5		8825	clocks	
D-PHY power-up	t6	1	1.1	ms	
D-PHY init	t7	100	110	µs	
After releasing software standby to data streaming time	t8	1.5 ms + exposure time			
Quick launch up time	t9		1	frame	stable time until optimal image quality

3-4.5 Power-down Sequence

Perform the power-off in the sequence shown below.

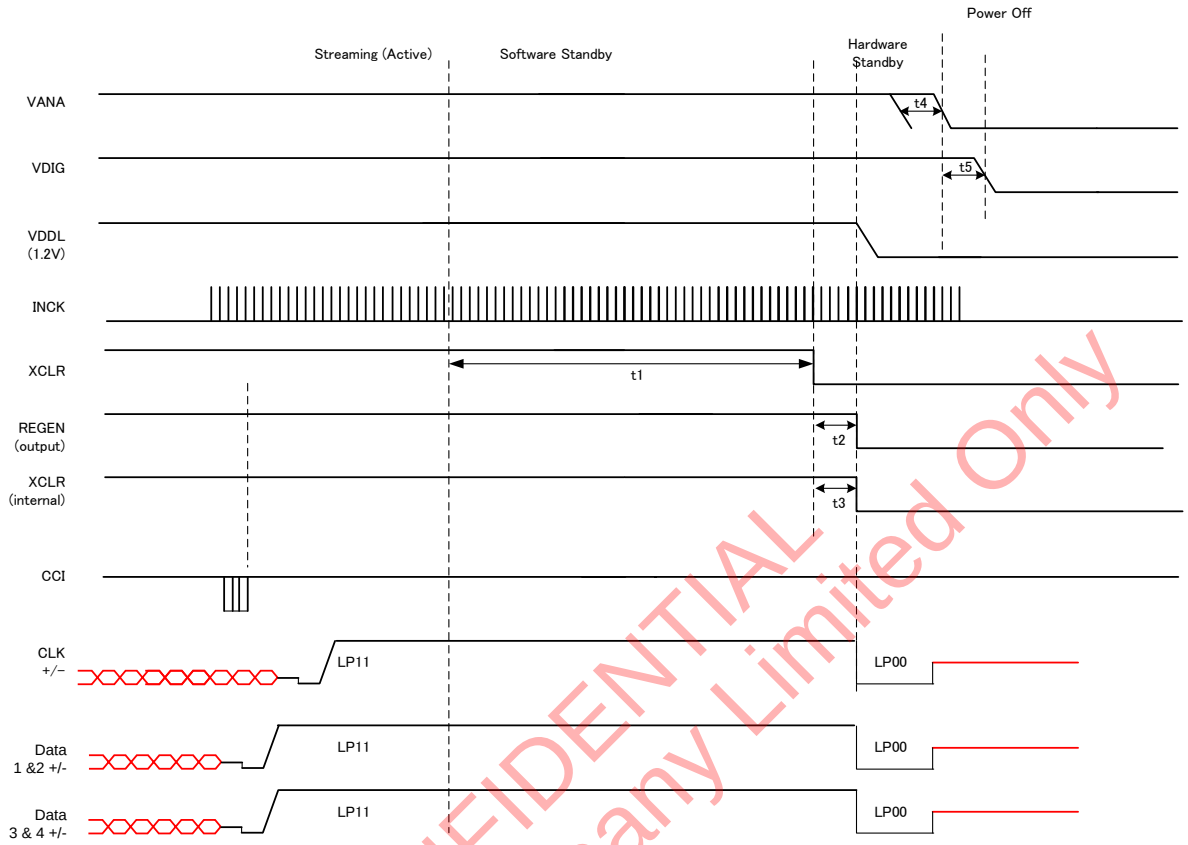


Fig. 20 Power-down Sequence in 2-wire Serial Communication

Table. 11 Operation Specifications in 2-wire Serial Communication

Constraint	Label	Min.	Max.	Units	Comment
Internal POR negedge - VANA (VDIG) fall	t1	0		ns	
Falling time of REGEN after XCLR H → L	t2		0.5	µs	
Falling time of internal XCLR after XCLR H → L	t3		0.5	µs	
VANA falling – VDIG falling	t4	VANA and VDIG may fall in any order.		ns	
VDIG falling – VANA falling	t5			ns	

T0 in power-off sequence varies depending on the CCI communication end timing as shown below.

1. When the CCI communication is performed with Software Standby between SOF and EOF, all communicated frame data is output and the status is converted to Software Standby.

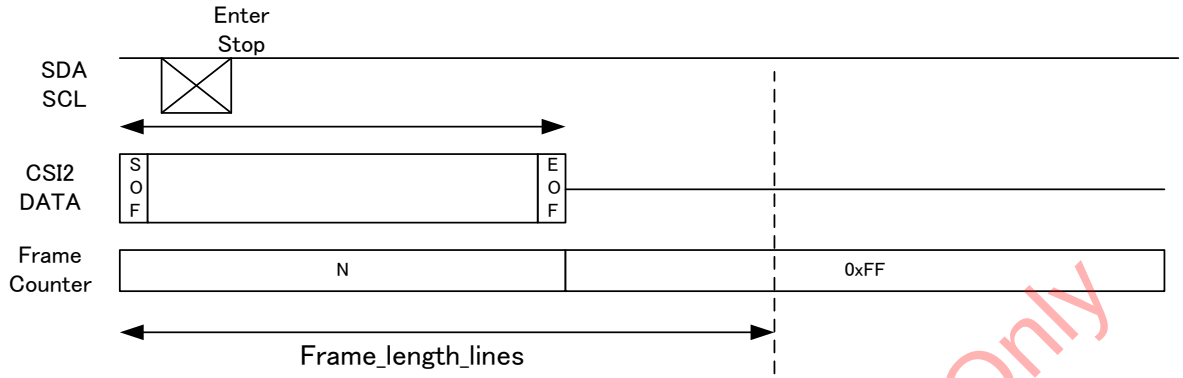


Fig. 21 Software Standby Operation Pattern 1

2. When the CCI communication is performed with Software Standby during FrameBlanking, the status is converted to Software Standby immediately after communication.

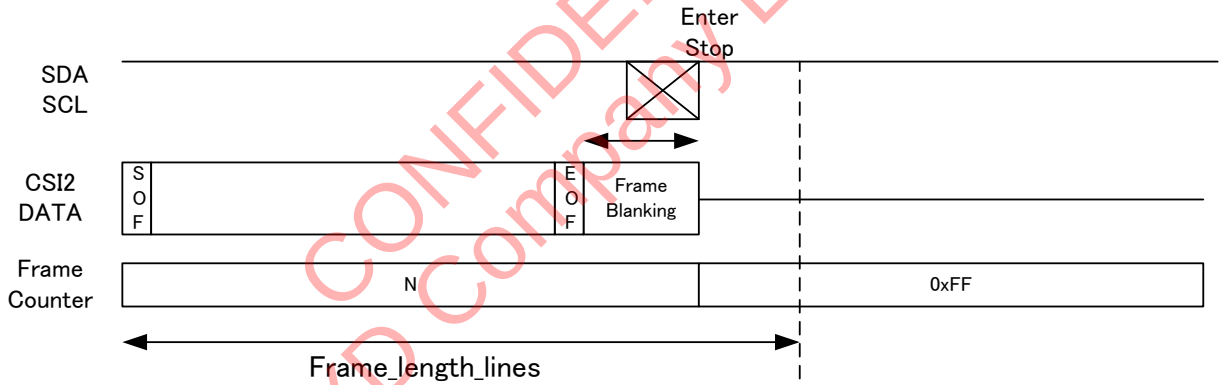


Fig. 22 Software Standby Operation Pattern 2

4. Output Data Format

4-1 CSI-2 Output Data Format

4-1.1 CSI-2 Output Data Channels

The IMX179 can select the CSI-2 2 lanes or CSI-2 4 lanes serial signal output method that uses all pairs of differential signals for image data output.

4-1.2 CSI-2 Frame Format

The data format of each line is based on CSI-2 General Frame Format.
The period from a line end sync code to the line start sync code for the next line is called the line blanking period. Likewise, the period from a frame end sync code to the next frame start sync code is called the frame blanking period.
Packet header consists of the following data.

Table. 12 Sync Code Settings

Header [7:0]	Description	Setting register	Remarks
[7:6]	Virtual Channel Identifier	Addr: 0x3360 CSI_channel_identifier	See Register Section
[5:0]	Synch Short Packet Data types	NA	
6'h00	Frame Start Code	NA	
6'h01	Frame End Code	NA	
6'h12	Embedded Data	NA	Written data in the sensor
6'h2A	RAW8	CSI_data_format	16'h0808
6'h2B	RAW10	CSI_data_format	16'h0A0A

4-1.2.1 CSI-2 Frame Structure

The image frame structure is shown below.

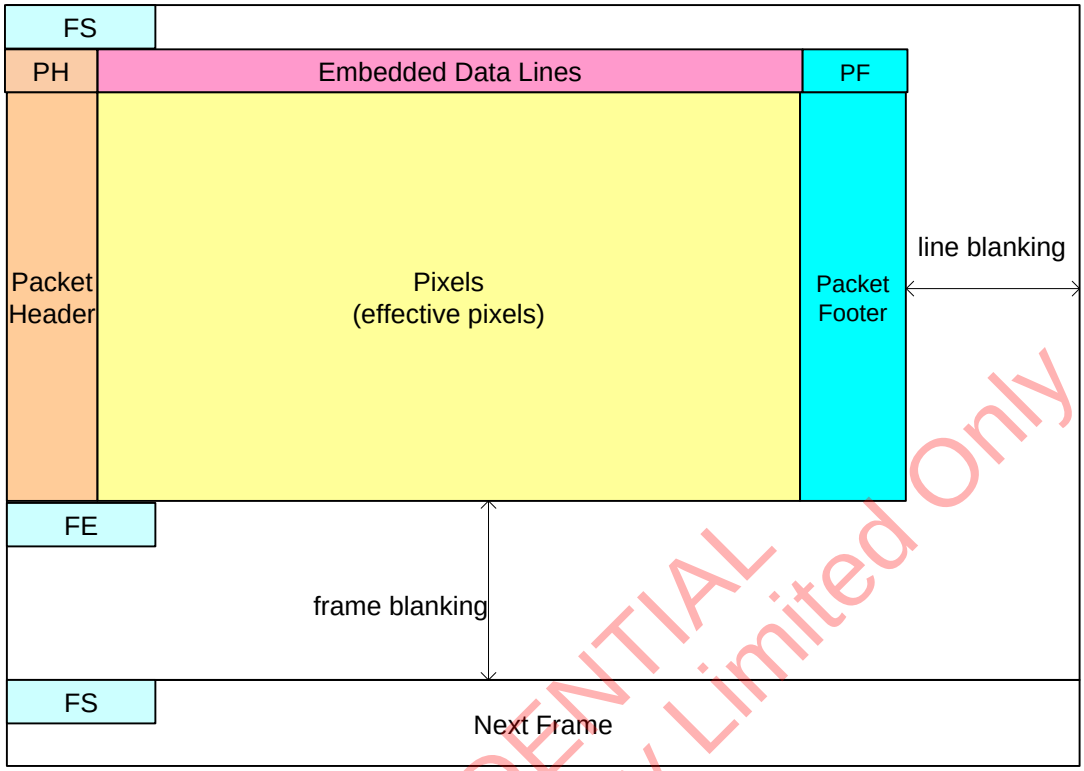


Fig. 23 Frame Structure for 2Lane Serial signal output

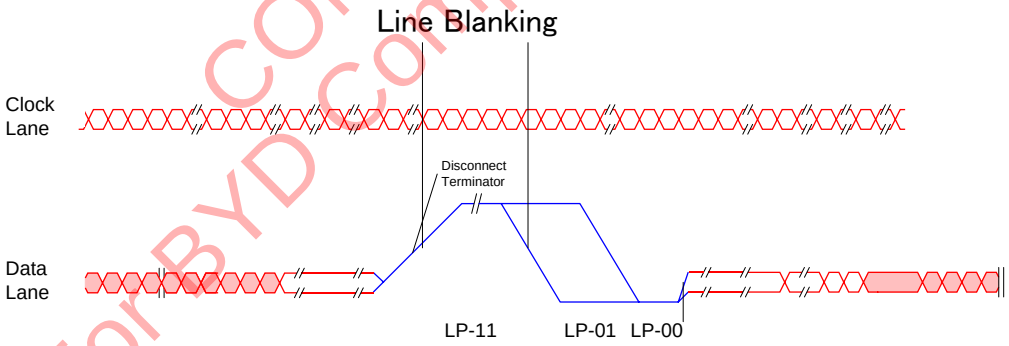


Fig. 24 Signaling Waveform during Line Blanking Period (CSI-2)

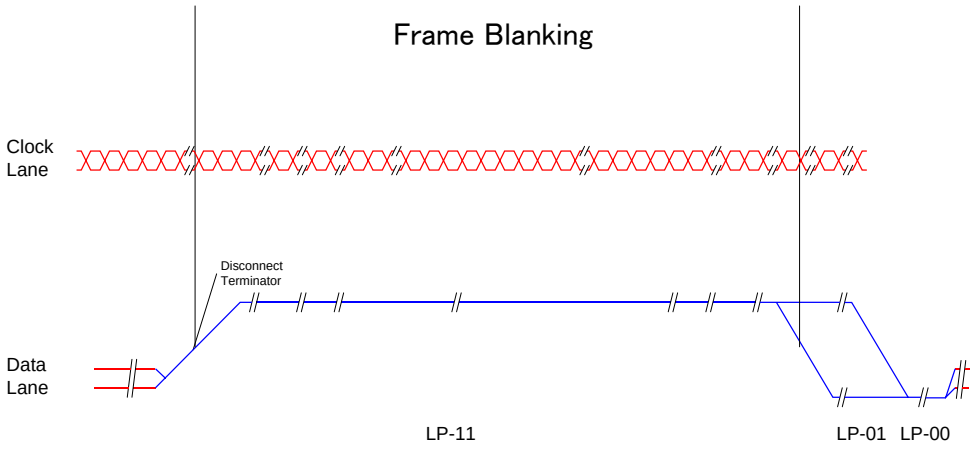


Fig. 25 Signaling Waveform during Frame Blanking Period (CSI-2)

4-1.3 CSI-2 Embedded Data Line

The value of the 2-wire serial communication configuration register can be output at the start of the frame. The output register is indicated in the “Embd DL” column of the 2-wire serial communication Register Map.
The Embedded data line is output in the two lines following the sync code FS.

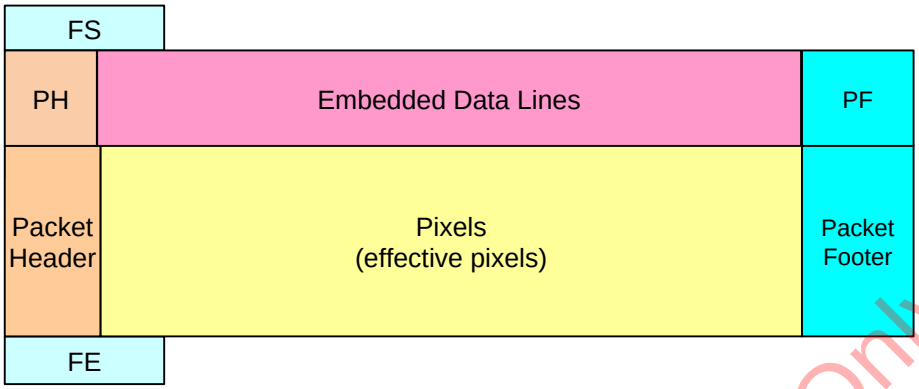


Fig. 26 Frame Format during Embedded Data Line Output

The output method differs according to the data format. In RAW10 mode, dummy bytes are inserted after outputting 4 bytes of data and tags.

RAW8 (top 8 bits, 10b-8b compress) mode Simplified 2-Byte Tagged Data Format

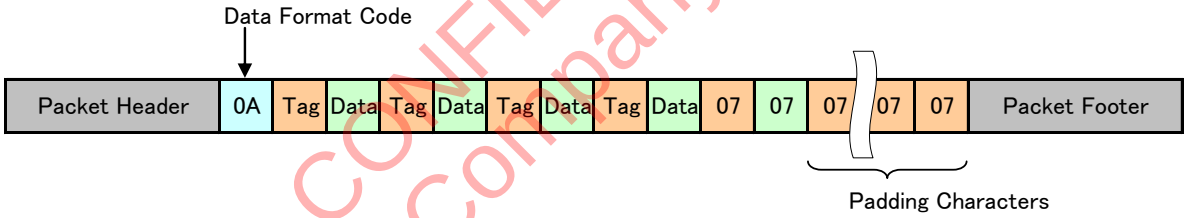


Fig. 27 Detailed Embedded Data Line Output in RAW8 Output Mode

RAW10 mode Simplified 2-Byte Tagged Data Format

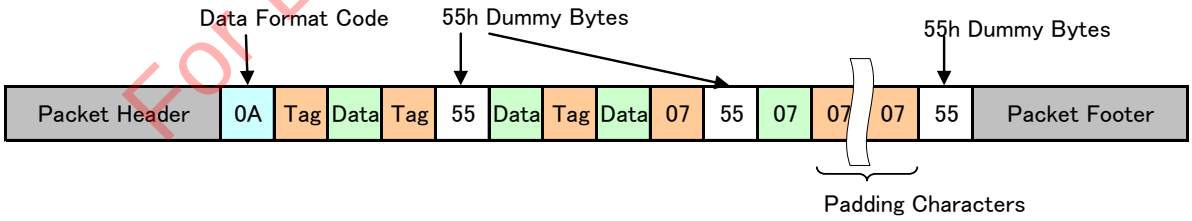


Fig. 28 Detailed Embedded Data Line Output in RAW10 Output Mode

The end of the address and register value is determined according to the tags embedded in the data.

Table. 13 Embedded Data Line Tag

Tag	Data Byte Description
00h	Illegal Tag. If found treat as end of Data
07h	End of Data (Data Byte Value = 07H)
aah	CCI Register Index MSB [15:8]
a5h	CCI Register Index LSB [7:0]
5ah	Auto increment the CCI index after the data byte - valid data Data byte contains valid CCI register data
55h	Auto increment the CCI index after the data byte - null data A CCI register does NOT exist for the current CCI index. The data byte value is the 07H
ffh	Illegal Tag. If found treat as end of Data

Registers

Specific output examples are shown on the following pages.

Addr (Hex)	Register Name	Description	in Byte (Hex)
0x0000	Fabrication	fab_rev_id	11
0x0001	Lot_ID[39:32]	[7:4]: FAB ID [3:0]: Revision ID of the Type (IMX179ES) Lot_ID of the sensor	29
0x0002	Lot_ID[31:24]		81
0x0003	Lot_ID[23:16]		79
0x0004	Lot_ID[15:8]		E1
0x0005	Lot_ID[7:0]		40
0x0006	—		00
0x0007	Wafer_Num	Wafer Number of the Sensor in the Lot. Value 0x01-0x19 is available.	25
0x0008	Chip_Number[15:8]	Chip ID in the wafer	15
0x0009	Chip_Number[7:0]		49
0x000A	Module_Date[15:8]	Module Production Date and NVM version [15:13]: NVM version [12:9]: Production Year (least two digits) [8:3]: work week (1 to 53) [2:0]: Day in the week. 1 (Monday) to 7 (Sunday)	00
0x000B	Module_Date[7:0]		00
0x000C	—		00
0x000D	Module_Serial_ID[23:16]	Serial ID of the Module	00
0x000E	Module_Serial_ID[15:8]		00
0x000F	Module_Serial_ID[7:0]		00
0x0010	Module_Parts_ID[15:8]	Module Parts ID [15]: Reserved [14:12]: Actuator ID [11:10]: Lens ID [9:8]: Integrator ID [7:2]: Reserved [1:0]: Driver ID	00
0x0011	Module_Parts_ID[7:0]		00
0x0012	FRM_CNT[7:0]	frame_count	FF
0x0013	PX_ORDER	pixel_order	1
0x0014	DT_PEDESTAL[9:8]	data_pedestal	40
0x0015	DT_PEDESTAL[7:0]		
0x0016	PIXEL_DEPTH	pixel_depth	A
0x0040	FRM_FMT_TYPE[7:0]	frame_format_model_type	01
0x0041	FRM_FMT_SUBTYPE[7:0]	frame_format_model_subtype	12
0x0042	FRM_FMT_DESC0[15:8]	frame_format_descriptor_0	5C
0x0043	FRM_FMT_DESC0[7:0]		D0
0x0044	FRM_FMT_DESC1[15:8]	frame_format_descriptor_1	10
0x0045	FRM_FMT_DESC1[7:0]		02

Addr (Hex)	Register Name	Description	in Byte (Hex)
0x0046	FRM_FMT_DESC2[15:8]	frame_format_descriptor_2	59
0x0047	FRM_FMT_DESC2[7:0]		A0
0x0080	—		00
0x0081	ANA_GAIN_CAPA	analogue_gain_capabiltiy	00
0x0084	—		00
0x0085	ANA_GAIN_Min.	analogue_gain_code_min	00
0x0086	ANA_GAIN_Max.[15:8]	analogue_gain_code_max	00
0x0087	ANA_GAIN_Max.[7:0]		E0
0x0088	ANA_GAIN_STEP[15:8]	analogue_gain_code_step	00
0x0089	ANA_GAIN_STEP[7:0]		01
0x008A	ANA_GAIN_TYPE[15:8]	analogue_gain_type	00
0x008B	ANA_GAIN_TYPE[7:0]		00
0x008C	ANA_GAIN_M0[15:8]	analogue_gain_m0	00
0x008D	ANA_GAIN_M0[7:0]		00
0x008E	ANA_GAIN_C0[15:8]	analogue_gain_c0	01
0x008F	ANA_GAIN_C0[7:0]		00
0x0090	ANA_GAIN_M1[15:8]	analogue_gain_m1	FF
0x0091	ANA_GAIN_M1[7:0]		FF
0x0092	ANA_GAIN_C1[15:8]	analogue_gain_c1	01
0x0093	ANA_GAIN_C1[7:0]		00
0x00C0	DT_FMT_TYPE[7:0]	data_format_model_type	01
0x00C1	DT_FMT_SUBTYPE[7:0]	data_format_model_subtype	03
0x00C2	DT_FMT_DESC0[15:8]	data_format_descriptor_0	08
0x00C3	DT_FMT_DESC0[7:0]		08
0x00C4	DT_FMT_DESC1[15:8]	data_format_descriptor_1	0A
0x00C5	DT_FMT_DESC1[7:0]		08
0x00C6	DT_FMT_DESC2[15:8]	data_format_descriptor_2	0A
0x00C7	DT_FMT_DESC2[7:0]		0A
0x0100	MODE_SEL	mode_select	00
0x0101	IMG_ORIENTATION[1:0]	image_orientation	00
0x0103	SW_RESET	software_reset	00
0x0202	COARSE_INTEG_TIME[15:8]	coarse_integration_time	09
0x0203	COARSE_INTEG_TIME[7:0]		AA
0x0204	—		00
0x0205	ANA_GAIN_GLOBAL	analogue_gain_code_global	E0
0x020E	DIG_GAIN_GR[11:8]	digital_gain_greenR	01
0x020F	DIG_GAIN_GR[7:0]		00

Addr (Hex)	Register Name	Description	in Byte (Hex)
0x0210	DIG_GAIN_R[11:8]	digital_gain_red	01
0x0211	DIG_GAIN_R[7:0]		00
0x0212	DIG_GAIN_B[11:8]	digital_gain_blue	01
0x0213	DIG_GAIN_B[7:0]		00
0x0214	DIG_GAIN_GB[11:8]	digital_gain_greenB	01
0x0215	DIG_GAIN_GB[7:0]		00
0x0340	FRM_LENGTH[15:8]	frame_length_lines	09
0x0341	FRM_LENGTH[7:0]		AE
0x0342	LINE_LENGTH[15:8]	line_length_pck	0D
0x0343	LINE_LENGTH[7:0]		70
0x0344	X_ADD_STA[11:8]	x_addr_start	00
0x0345	X_ADD_STA[7:0]		00
0x0346	Y_ADD_STA[11:8]	y_addr_start	00
0x0347	Y_ADD_STA[7:0]		00
0x0348	X_ADD_END[11:8]	x_addr_end	0C
0x0349	X_ADD_END[7:0]		CF
0x034A	Y_ADD_END[11:8]	y_addr_end	09
0x034B	Y_ADD_END[7:0]		9F
0x034C	X_OUT_SIZE[11:8]	x_output_size	0C
0x034D	X_OUT_SIZE[7:0]		D0
0x034E	Y_OUT_SIZE[11:8]	y_output_size	09
0x034F	Y_OUT_SIZE[7:0]		A0
0x0380	—		00
0x0381	X_EVN_INC	x_even_inc	01
0x0382	—		00
0x0383	X_ODD_INC	x_odd_inc	01
0x0384	—		00
0x0385	Y_EVN_INC	y_even_inc	01
0x0386	—		00
0x0387	Y_ODD_INC	y_odd_inc	01
0x0390	BINNING_MODE	defines binning mode. 0:no-binning 1:2x2-binning 2:4x4-binning	00
0x0301	VTPXCK_DIV	vt_pix_clk_div	05
0x0303	VTSYCK_DIV	vt_sys_clk_div	01
0x0305	PREPLLCK_ DIV	pre_pll_clk _div	0B
0x0309	OPPXCK_DIV	op_pix_clk_div	05
0x030B	OPSYCK_DIV	op_sys_clk_div	01

Addr (Hex)	Register Name	Description	in Byte (Hex)
0x030C	PLL_ MPY[10:8]	pll_ multiplier	0
0x030D	PLL_ MPY[7:0]		A0
0x0401	SCALE_MODE	Scaling_mode	00
0x0404	SCALE_M[8]	scale_m	00
0x0405	SCALE_M[7:0]		10
0x0407	SCALE_N	scale_n	10
0x0600	TP_MODE[8]	test_pattern_mode	00
0x0601	TP_MODE[7:0]		00
0x0602	TD_R[9:8]	test_data_red	00
0x0603	TD_R[7:0]		00
0x0604	TD_GR[9:8]	test_data_greenR	00
0x0605	TD_GR[7:0]		00
0x0606	TD_B[9:8]	test_data_blue	00
0x0607	TD_B[7:0]		00
0x0608	TD_GB[9:8]	test_data_greenB	00
0x0609	TD_GB[7:0]		00
0x060A	H_CUR_WIDTH[15:8]	horizontal_cursor_width	00
0x060B	H_CUR_WIDTH[7:0]		00
0x060C	H_CUR_POS[15:8]	horizontal_cursor_position	00
0x060D	H_CUR_POS[7:0]		00
0x060E	V_CUR_WIDTH[15:8]	vertical_cursor_width	00
0x060F	V_CUR_WIDTH[7:0]		00
0x0610	V_CUR_POS[15:8]	vertical_cursor_position	00
0x0611	V_CUR_POS[7:0]		00

5. Setting Required for Imaging

5-1 Pixel Array Physical Image

Pixel array physical image is shown below. It is the pixel array when upper left corner of the physical image is Pin 1. The IMX179 has vertical OB area, which cannot read out.

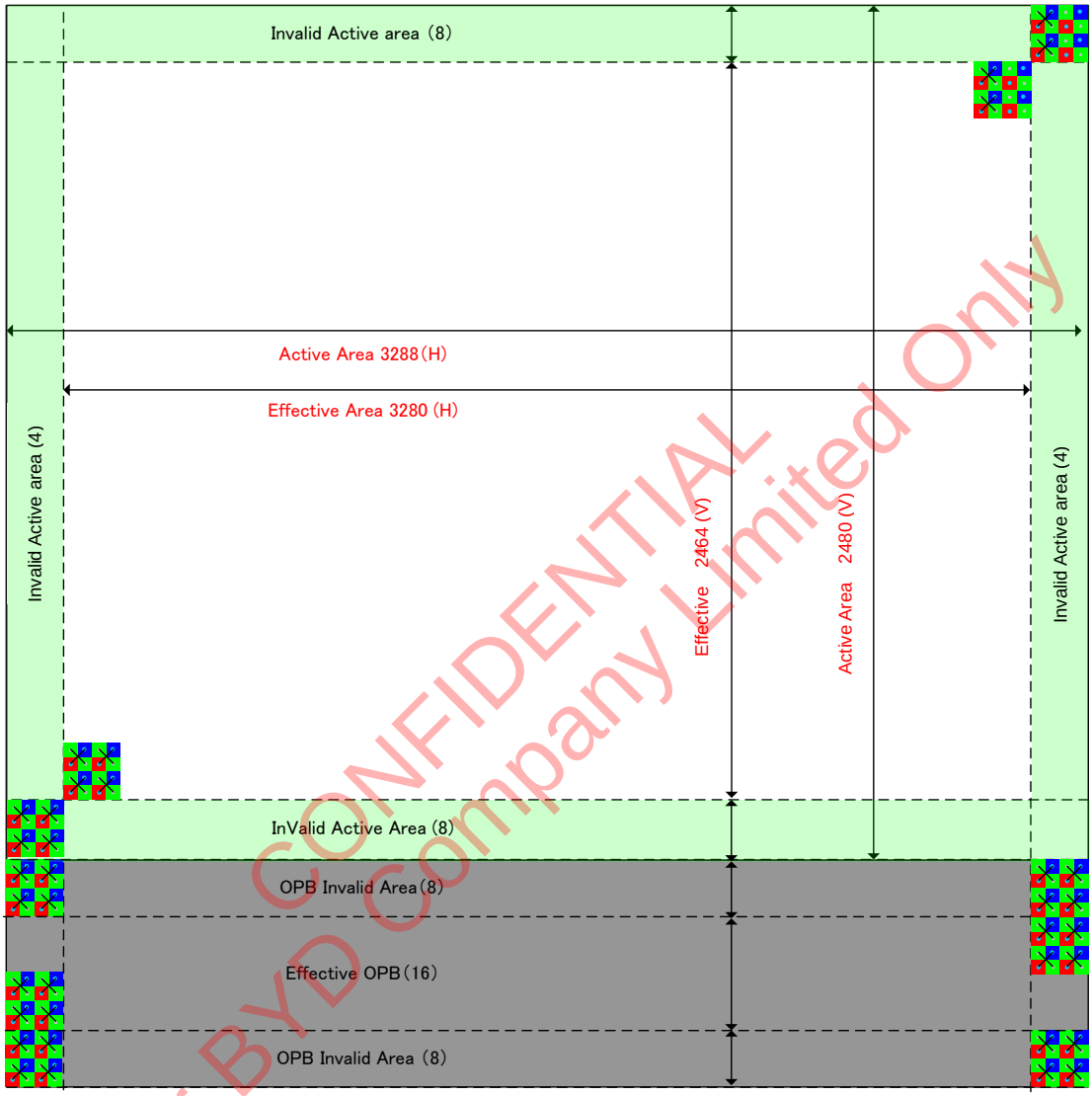


Fig. 29 Pixel Array Physical Image

5-2 Pixel Binning Mode

Binning read-out can be used to obtain an image of lower resolution for full field of view. It has advantage on frame rate than using digital scaling, and on signal-to-noise ratio than using sub-sampling. See Binning Capability Registers, for detail of available configurations.
The following diagram describes on 2x2 averaged binning operations. Pixels of two adjacent rows and columns are averaged, and read out as one output pixel.

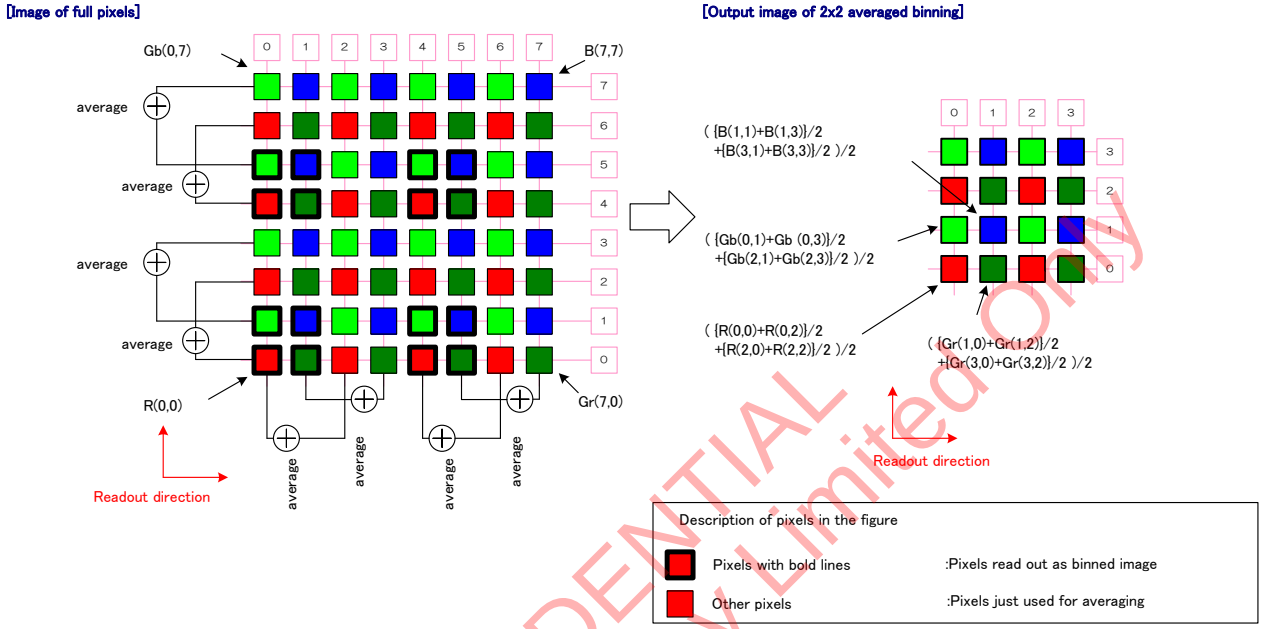


Fig. 30 Image of 2x2 averaged Binning Mode

For explanation, represent individual pixels with its addresses in the format “color (x, y) ” - for example, The Red pixel in the lower left corner is expressed as R (0, 0).
By performing 2x2 binning, R (0, 0) after binning is obtained by the following equation.

$$R\ (0,\ 0)\ \text{after binning} = (\ \{R\ (0,\ 0) + R\ (0,\ 2)\}\ /2 + \{R\ (2,0) + R\ (2,2)\}\ /2\ )\ /\ 2$$

And, the total number of output pixels is reduced to 1/4 of the original pixel array.

5-3 Readout Position

The IMX179 default status is readout from the lower left corner when Pin 1 is located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin 1 is located in the upper left corner.

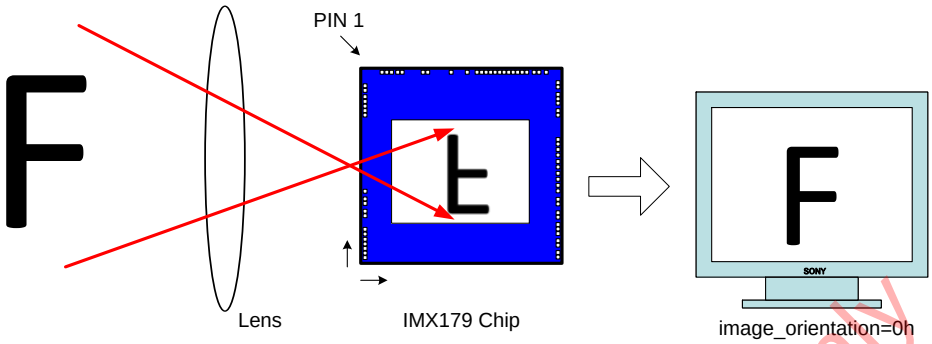


Fig. 31 Readout Position

Readout direction can be set by the registers.

Table. 14 Image Orientation Register

CCI register	image_orientation 0x0101 [0]	Mode
	0	no mirror (Readout from the left with Pin 1 in the upper left corner)
	1	Horizontal Mirror (Readout from the right with Pin 1 in the upper left corner)
	image_orientation 0x0101 [1]	Mode
	0	no flip (Readout from the bottom with Pin 1 in the upper left corner)
	1	Vertical Flip (Readout from the top with Pin 1 in the upper left corner)

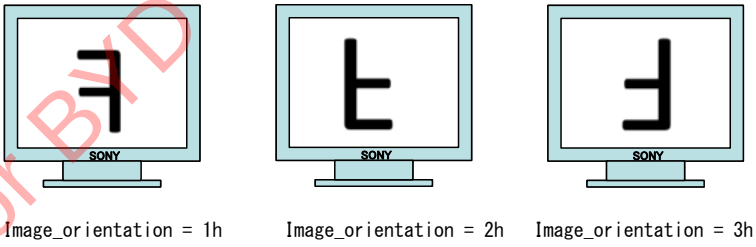


Fig. 32 Output Image Diagrams for Vertical Flip and Horizontal Mirror

5-4 Frame Rate Calculation Formula

Frame rate is calculated by the followings.

$$Frame\_Rate[fps] = \frac{1}{Time\_per\_Line[sec] \times (Frame\_Length)}$$

$$Time\_Per\_Line[sec] = \frac{Line\_Length\_pck[pix]}{2 \times Pix\_Clock\_Freq[MHz]}$$

5-5 Black Level Control

The IMX179 has a stable black level clamp function. The average value of the black level is adjusted to 64d.
When selecting output format RAW8 (uncompressed), Black level in the table below is divided by 4.

Table. 15 Black Level

	Black Level (dec)
CCI	64 (Fixed)

5-6 Storage Time (Electronic Shutter) Settings

5-6.1 Storage Time (Electronic Shutter) Setting Registers

The storage time setting registers are shown below. The value of the register, coarse_integration_time, indicates the number of lines for the storage time.
The maximum storage time value is obtained by subtracting “4” from the number of lines per frame (set by coarse_integration_time) including the blanking period.

Table. 16 Storage Time Setting Register

	Register name	Address	Setting value (dec)	Remarks
CCI registers	coarse_integration_time	0x0202 0x0203	1 to frame_length_lines-4	0x0202 = coarse_integration_time[15:8] 0x0203 = coarse_integration_time[7:0]

The value of the register, fine_integration_time, indicates the number of pixels for the storage time.
The register, fine_integration_time, is a fixed value, read only register.

Table. 17 Storage Time Offset Register

	Register name	Address	Setting value (dec)	Remarks
CCI registers	fine_integration_time	0x0200 0x0201	488	RO register

5-6.2 Storage Time Calculation Method

The storage time (T_{SH}) can be obtained from the following equation.

$$T_{SH} = (Coarse\_Inregtation\_Time \times Line\_Length\_Pck + \alpha) \times pix\_clk\_period$$

Where α = offset time = readdable from fine_integration_time register.
pix_clk_period [s] = 1 / CK_PIXEL.
CK_PIXEL = EXTCLK frequency × (pll_multiplier / pre_pll_clk_div) / (vt_sys_clk_div × vt_pix_clk_div) × 2.

Table. 18 Storage Time Setting (in case of Line_Length_PCK = 3600)

	Number of total lines	frame_length_lines [15:0]	coarse_integration_time [15:0]	Storage time (T_{SH})
	Dec	Dec	Dec	All-pixel scan [s]
Normal frame rate	2592	2592	1	(1 x 3600 + 488) x pix_clk_period
			N	(N x 3600 + 488) x pix_clk_period
			:	:
			2588	(2588 x 3600 + 488) x pix_clk_period
Low frame rate Long-time exposure	2593	2593	2589	(2589 x 3600 + 488) x pix_clk_period
	2594	2594	2590	(2590 x 3600 + 488) x pix_clk_period
	:	:	:	:
	M + 4	M + 4	M	(M x 3600 + 488) x pix_clk_period
	:	:	:	:
	65535	65535	65531	(65531 x 3600 + 488) x pix_clk_period

5-7 Gain Settings

Analogue gain and digital gain can be set independently.

5-7.1 Analogue Gain Settings

Only global analogue gain is supported.
The analogue gain is set by the following equation.

$$Gain\_analogue = \frac{(m0 \times X + c0)}{(m1 \times X + c1)}$$

The variables are shown in the table below.

Table. 19 Gain Setting Variables

		Register name	Address	Remarks
CCI registers	m0	analogue_gain_m0	0x008C/0x008D	Fixed to 0
	m1	analogue_gain_m1	0x0090/0x0091	Fixed to -1
	c0	analogue_gain_c0	0x008E/0x008F	Fixed to 256
	c1	analogue_gain_c1	0x0092/0x0093	Fixed to 256
	X	analogue_gain_code_global	0x0204/0x0205	0 to 224

Therefore, the analogue gain is as follows.

$$Gain\_analogue = \frac{(256)}{(256 - X)}$$

The relationship between the setting value X (analogue_gain_code_global) and the gain is shown on the following page.

Table. 20 Analogue Gain Setting

analogue_gain_code_global	Gain(times)	Gain(dB)	analogue_gain_code_global	Gain(times)	Gain(dB)	analogue_gain_code_global	Gain(times)	Gain(dB)	analogue_gain_code_global	Gain(times)	Gain(dB)	analogue_gain_code_global	Gain(times)	Gain(dB)
0	1.00	0.00	45	1.21	1.68	90	1.54	3.76	135	2.12	6.51	180	3.37	10.55
1	1.00	0.03	46	1.22	1.72	91	1.55	3.82	136	2.13	6.58	181	3.41	10.66
2	1.01	0.07	47	1.22	1.76	92	1.56	3.87	137	2.15	6.65	182	3.46	10.78
3	1.01	0.10	48	1.23	1.80	93	1.57	3.92	138	2.17	6.73	183	3.51	10.90
4	1.02	0.14	49	1.24	1.85	94	1.58	3.97	139	2.19	6.80	184	3.56	11.02
5	1.02	0.17	50	1.24	1.89	95	1.59	4.03	140	2.21	6.88	185	3.61	11.14
6	1.02	0.21	51	1.25	1.93	96	1.60	4.08	141	2.23	6.95	186	3.66	11.26
7	1.03	0.24	52	1.25	1.97	97	1.61	4.14	142	2.25	7.03	187	3.71	11.39
8	1.03	0.28	53	1.26	2.01	98	1.62	4.19	143	2.27	7.10	188	3.76	11.51
9	1.04	0.31	54	1.27	2.06	99	1.63	4.25	144	2.29	7.18	189	3.82	11.64
10	1.04	0.35	55	1.27	2.10	100	1.64	4.30	145	2.31	7.26	190	3.88	11.77
11	1.04	0.38	56	1.28	2.14	101	1.65	4.36	146	2.33	7.34	191	3.94	11.91
12	1.05	0.42	57	1.29	2.19	102	1.66	4.41	147	2.35	7.42	192	4.00	12.04
13	1.05	0.45	58	1.29	2.23	103	1.67	4.47	148	2.37	7.50	193	4.06	12.18
14	1.06	0.49	59	1.30	2.28	104	1.68	4.53	149	2.39	7.58	194	4.13	12.32
15	1.06	0.52	60	1.31	2.32	105	1.70	4.59	150	2.42	7.66	195	4.20	12.46
16	1.07	0.56	61	1.31	2.36	106	1.71	4.64	151	2.44	7.74	196	4.27	12.60
17	1.07	0.60	62	1.32	2.41	107	1.72	4.70	152	2.46	7.82	197	4.34	12.75
18	1.08	0.63	63	1.33	2.45	108	1.73	4.76	153	2.49	7.91	198	4.41	12.90
19	1.08	0.67	64	1.33	2.50	109	1.74	4.82	154	2.51	7.99	199	4.49	13.05
20	1.08	0.71	65	1.34	2.54	110	1.75	4.88	155	2.53	8.08	200	4.57	13.20
21	1.09	0.74	66	1.35	2.59	111	1.77	4.94	156	2.56	8.16	201	4.65	13.36
22	1.09	0.78	67	1.35	2.64	112	1.78	5.00	157	2.59	8.25	202	4.74	13.52
23	1.10	0.82	68	1.36	2.68	113	1.79	5.06	158	2.61	8.34	203	4.83	13.68
24	1.10	0.86	69	1.37	2.73	114	1.80	5.12	159	2.64	8.43	204	4.92	13.84
25	1.11	0.89	70	1.38	2.77	115	1.82	5.18	160	2.67	8.52	205	5.02	14.01
26	1.11	0.93	71	1.38	2.82	116	1.83	5.24	161	2.69	8.61	206	5.12	14.19
27	1.12	0.97	72	1.39	2.87	117	1.84	5.30	162	2.72	8.70	207	5.22	14.36
28	1.12	1.01	73	1.40	2.92	118	1.86	5.37	163	2.75	8.80	208	5.33	14.54
29	1.13	1.04	74	1.41	2.96	119	1.87	5.43	164	2.78	8.89	209	5.45	14.72
30	1.13	1.08	75	1.41	3.01	120	1.88	5.49	165	2.81	8.98	210	5.57	14.91
31	1.14	1.12	76	1.42	3.06	121	1.90	5.56	166	2.84	9.08	211	5.69	15.10
32	1.14	1.16	77	1.43	3.11	122	1.91	5.62	167	2.88	9.18	212	5.82	15.30
33	1.15	1.20	78	1.44	3.16	123	1.92	5.69	168	2.91	9.28	213	5.95	15.50
34	1.15	1.24	79	1.45	3.21	124	1.94	5.75	169	2.94	9.37	214	6.10	15.70
35	1.16	1.28	80	1.45	3.25	125	1.95	5.82	170	2.98	9.47	215	6.24	15.91
36	1.16	1.32	81	1.46	3.30	126	1.97	5.89	171	3.01	9.58	216	6.40	16.12
37	1.17	1.36	82	1.47	3.35	127	1.98	5.95	172	3.05	9.68	217	6.56	16.34
38	1.17	1.40	83	1.48	3.40	128	2.00	6.02	173	3.08	9.78	218	6.74	16.57
39	1.18	1.44	84	1.49	3.45	129	2.02	6.09	174	3.12	9.89	219	6.92	16.80
40	1.19	1.48	85	1.50	3.50	130	2.03	6.16	175	3.16	10.00	220	7.11	17.04
41	1.19	1.52	86	1.51	3.56	131	2.05	6.23	176	3.20	10.10	221	7.31	17.28
42	1.20	1.56	87	1.51	3.61	132	2.06	6.30	177	3.24	10.21	222	7.53	17.54
43	1.20	1.60	88	1.52	3.66	133	2.08	6.37	178	3.28	10.32	223	7.76	17.79
44	1.21	1.64	89	1.53	3.71	134	2.10	6.44	179	3.32	10.43	224	8.00	18.06

5-7.2 Digital gain settings

The IMX179 can set the digital gain for each color. The registers required to set the digital gain are as follows.

Table. 21 Digital Gain Settings

CCI register name	Upper byte address (Setting range:1 to15)	Lower byte address (Setting range:0 to 255)
digital_gain_greenR (GR)	0x020E	0x020F
digital_gain_red (R)	0x0210	0x0211
digital_gain_blue (B)	0x0212	0x0213
digital_gain_greenB (GB)	0x0214	0x0215

Each register is comprised of 2 bytes, with the upper byte [15:8] setting the integer portion and the lower byte [7:0] setting the fractional portion of the gain. The gain for each color is obtained by the following equation.

$$\text{Gain\_digital} = \text{Upper byte} + \frac{\text{Lower byte}}{256}$$

The upper byte can be set to a value between 1 and 15, and the lower byte to a value between 0 and 255. Therefore, the digital gain setting range for each color is as follows.

$$1 + \frac{0}{256}\ [\text{times}](0\text{dB}) \le \text{Gain\_digital} \le 15 + \frac{255}{256}\ [\text{times}](24\text{dB})$$

When gain is considered in log linear scale, the adjustment steps are large at low gain and extremely small at high gain. The register values are shown on the following page in case of the gain in log linear manner in 0.1 dB steps.

Table. 22 Example of Digital Gain Setting

Upper byte		Lower byte		Gain(times)	Gain(dB)
dec	hex	dec	hex		
1	1	0	0	1.00	0.00
1	1	3	3	1.01	0.10
1	1	6	6	1.02	0.20
1	1	9	9	1.04	0.30
1	1	12	C	1.05	0.40
1	1	15	F	1.06	0.49
1	1	18	12	1.07	0.59
1	1	21	15	1.08	0.68
1	1	25	19	1.10	0.81
1	1	28	1C	1.11	0.90
1	1	31	1F	1.12	0.99
1	1	35	23	1.14	1.11
1	1	38	26	1.15	1.20
1	1	41	29	1.16	1.29
1	1	45	2D	1.18	1.41
1	1	48	30	1.19	1.49
1	1	52	34	1.20	1.61
1	1	55	37	1.21	1.69
1	1	59	3B	1.23	1.80
1	1	63	3F	1.25	1.91
1	1	66	42	1.26	1.99
1	1	70	46	1.27	2.10
1	1	74	4A	1.29	2.21
1	1	78	4E	1.30	2.31
1	1	81	51	1.32	2.39
1	1	85	55	1.33	2.49
1	1	89	59	1.35	2.59
1	1	93	5D	1.36	2.69
1	1	97	61	1.38	2.79
1	1	101	65	1.39	2.89
1	1	106	6A	1.41	3.01
1	1	110	6E	1.43	3.10
1	1	114	72	1.45	3.20
1	1	118	76	1.46	3.29
1	1	123	7B	1.48	3.41
1	1	127	7F	1.50	3.50
1	1	131	83	1.51	3.59
1	1	136	88	1.53	3.70
1	1	140	8C	1.55	3.79
1	1	145	91	1.57	3.90
1	1	150	96	1.59	4.01
1	1	154	9A	1.60	4.09
1	1	159	9F	1.62	4.20
1	1	164	A4	1.64	4.30
1	1	169	A9	1.66	4.40
1	1	174	AE	1.68	4.50
1	1	179	B3	1.70	4.60
1	1	184	B8	1.72	4.70
1	1	189	BD	1.74	4.80
1	1	194	C2	1.76	4.90
1	1	199	C7	1.78	5.00
1	1	205	CD	1.80	5.11
1	1	210	D2	1.82	5.20
1	1	215	D7	1.84	5.30
1	1	221	DD	1.86	5.41
1	1	226	E2	1.88	5.50
1	1	232	E8	1.91	5.60
1	1	237	ED	1.93	5.69
1	1	243	F3	1.95	5.80
1	1	249	F9	1.97	5.90

Upper byte		Lower byte		Gain(times)	Gain(dB)
dec	hex	dec	hex		
1	1	255	FF	2.00	6.00
2	2	5	5	2.02	6.11
2	2	11	B	2.04	6.21
2	2	17	11	2.07	6.30
2	2	23	17	2.09	6.40
2	2	29	1D	2.11	6.50
2	2	35	23	2.14	6.59
2	2	42	2A	2.16	6.71
2	2	48	30	2.19	6.80
2	2	55	37	2.21	6.91
2	2	61	3D	2.24	7.00
2	2	68	44	2.27	7.10
2	2	74	4A	2.29	7.19
2	2	81	51	2.32	7.30
2	2	88	58	2.34	7.40
2	2	95	5F	2.37	7.50
2	2	102	66	2.40	7.60
2	2	109	6D	2.43	7.70
2	2	116	74	2.45	7.79
2	2	124	7C	2.48	7.90
2	2	131	83	2.51	8.00
2	2	138	8A	2.54	8.09
2	2	146	92	2.57	8.20
2	2	154	9A	2.60	8.30
2	2	161	A1	2.63	8.40
2	2	169	A9	2.66	8.50
2	2	177	B1	2.69	8.60
2	2	185	B9	2.72	8.70
2	2	193	C1	2.75	8.80
2	2	201	C9	2.79	8.90
2	2	210	D2	2.82	9.01
2	2	218	DA	2.85	9.10
2	2	226	E2	2.88	9.20
2	2	235	EB	2.92	9.30
2	2	244	F4	2.95	9.41
2	2	252	FC	2.98	9.50
3	3	5	5	3.02	9.60
3	3	14	E	3.05	9.70
3	3	23	17	3.09	9.80
3	3	32	20	3.13	9.90
3	3	42	2A	3.16	10.00
3	3	51	33	3.20	10.10
3	3	60	3C	3.23	10.20
3	3	70	46	3.27	10.30
3	3	80	50	3.31	10.40
3	3	90	5A	3.35	10.50
3	3	99	63	3.39	10.60
3	3	109	6D	3.43	10.70
3	3	120	78	3.47	10.80
3	3	130	82	3.51	10.90
3	3	140	8C	3.55	11.00
3	3	151	97	3.59	11.10
3	3	161	A1	3.63	11.20
3	3	172	AC	3.67	11.30
3	3	183	B7	3.71	11.40
3	3	194	C2	3.76	11.50
3	3	205	CD	3.80	11.60
3	3	217	D9	3.85	11.70
3	3	228	E4	3.89	11.80
3	3	239	EF	3.93	11.90

Upper byte		Lower byte		Gain(times)	Gain(dB)
dec	hex	dec	hex		
3	3	251	FB	3.98	12.00
4	4	7	7	4.03	12.10
4	4	19	13	4.07	12.20
4	4	31	1F	4.12	12.30
4	4	43	2B	4.17	12.40
4	4	56	38	4.22	12.50
4	4	68	44	4.27	12.60
4	4	81	51	4.32	12.70
4	4	93	5D	4.36	12.80
4	4	106	6A	4.41	12.90
4	4	120	78	4.47	13.00
4	4	133	85	4.52	13.10
4	4	146	92	4.57	13.20
4	4	160	A0	4.63	13.30
4	4	173	AD	4.68	13.40
4	4	187	BB	4.73	13.50
4	4	201	C9	4.79	13.60
4	4	215	D7	4.84	13.70
4	4	230	E6	4.90	13.80
4	4	244	F4	4.95	13.90
5	5	3	3	5.01	14.00
5	5	18	12	5.07	14.10
5	5	33	21	5.13	14.20
5	5	48	30	5.19	14.30
5	5	64	40	5.25	14.40
5	5	79	4F	5.31	14.50
5	5	95	5F	5.37	14.60
5	5	111	6F	5.43	14.70
5	5	127	7F	5.50	14.80
5	5	143	8F	5.56	14.90
5	5	160	A0	5.63	15.00
5	5	176	B0	5.69	15.10
5	5	193	C1	5.75	15.20
5	5	210	D2	5.82	15.30
5	5	227	E3	5.89	15.40
5	5	245	F5	5.96	15.50
6	6	7	7	6.03	15.60
6	6	24	18	6.09	15.70
6	6	42	2A	6.16	15.80
6	6	61	3D	6.24	15.90
6	6	79	4F	6.31	16.00
6	6	98	62	6.38	16.10
6	6	117	75	6.46	16.20
6	6	136	88	6.53	16.30
6	6	155	9B	6.61	16.40
6	6	175	AF	6.68	16.50
6	6	195	C3	6.76	16.60
6	6	215	D7	6.84	16.70
6	6	235	EB	6.92	16.80
7	7	0	0	7.00	16.90
7	7	20	14	7.08	17.00
7	7	41	29	7.16	17.10
7	7	63	3F	7.25	17.20
7	7	84	54	7.33	17.30
7	7	106	6A	7.41	17.40
7	7	128	80	7.50	17.50
7	7	150	96	7.59	17.60
7	7	172	AC	7.67	17.70
7	7	195	C3	7.76	17.80
7	7	218	DA	7.85	17.90

Upper byte		Lower byte		Gain(times)	Gain(dB)
dec	hex	dec	hex		
7	7	241	F1	7.94	18.00
8	8	9	9	8.04	18.10
8	8	33	21	8.13	18.20
8	8	57	39	8.22	18.30
8	8	81	51	8.32	18.40
8	8	106	6A	8.41	18.50
8	8	131	83	8.51	18.60
8	8	156	9C	8.61	18.70
8	8	182	B6	8.71	18.80
8	8	207	CF	8.81	18.90
8	8	234	EA	8.91	19.00
9	9	4	4	9.02	19.10
9	9	31	1F	9.12	19.20
9	9	58	3A	9.23	19.30
9	9	85	55	9.33	19.40
9	9	113	71	9.44	19.50
9	9	141	8D	9.55	19.60
9	9	169	A9	9.66	19.70
9	9	198	C6	9.77	19.80
9	9	227	E3	9.89	19.90
10	A	0	0	10.00	20.00
10	A	30	1E	10.12	20.10
10	A	60	3C	10.23	20.20
10	A	90	5A	10.35	20.30
10	A	121	79	10.47	20.40
10	A	152	98	10.59	20.50
10	A	183	B7	10.71	20.60
10	A	215	D7	10.84	20.70
10	A	247	F7	10.96	20.80
11	B	23	17	11.09	20.90
11	B	56	38	11.22	21.00
11	B	90	5A	11.35	21.10
11	B	123	7B	11.48	21.20
11	B	157	9D	11.61	21.30
11	B	192	C0	11.75	21.40
11	B	227	E3	11.89	21.50
12	C	6	6	12.02	21.60
12	C	41	29	12.16	21.70
12	C	77	4D	12.30	21.80
12	C	114	72	12.45	21.90
12	C	151	97	12.59	22.00
12	C	188	BC	12.73	22.10
12	C	226	E2	12.88	22.20
13	D	8	8	13.03	22.30
13	D	47	2F	13.18	22.40
13	D	86	56	13.34	22.50
13	D	125	7D	13.49	22.60
13	D	165	A5	13.64	22.70
13	D	206	CE	13.80	22.80
13	D	247	F7	13.96	22.90
14	E	32	20	14.13	23.00
14	E	74	4A	14.29	23.10
14	E	116	74	14.45	23.20
14	E	159	9F	14.62	23.30
14	E	203	CB	14.79	23.40
14	E	246	F6	14.96	23.50
15	F	35	23	15.14	23.60
15	F	80	50	15.31	23.70
15	F	125	7D	15.49	23.80
15	F	171	AB	15.67	23.90
15	F	217	D9	15.85	24.00

6. On Chip Image Processing

Data flow of our “On-Chip Image Processing” is written in following figure.
A/D-converted digital signal is input, and processed data is asserted from CSI-2.

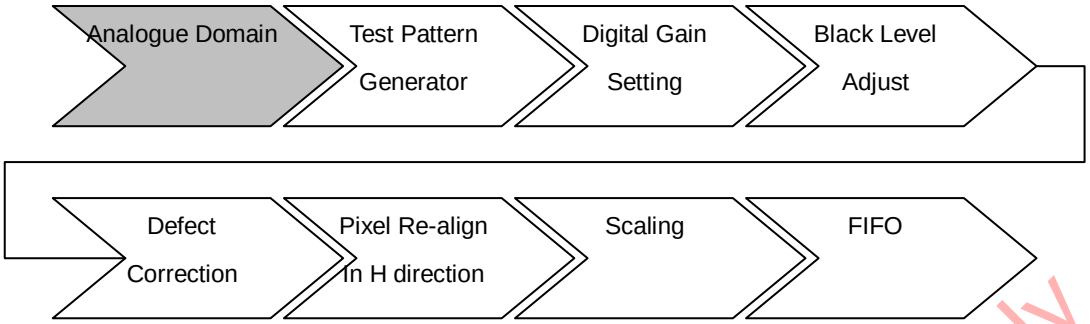


Fig. 33 Data Flow Diagram

6-1 Test Pattern Generator

The IMX179 can output test signals using the internal pattern generator.

6-1.1 Test Pattern

The test pattern output function outputs fixed pattern image data from the IMX179. Built-in image patterns can be output by setting the necessary registers.
The registers must be set by communication to output the test pattern. There are no restrictions on the sequence for setting the registers related to test pattern output. The prescribed output is obtained by setting the necessary registers while the sensor is operating.

Table. 23 Description of Test Pattern Registers

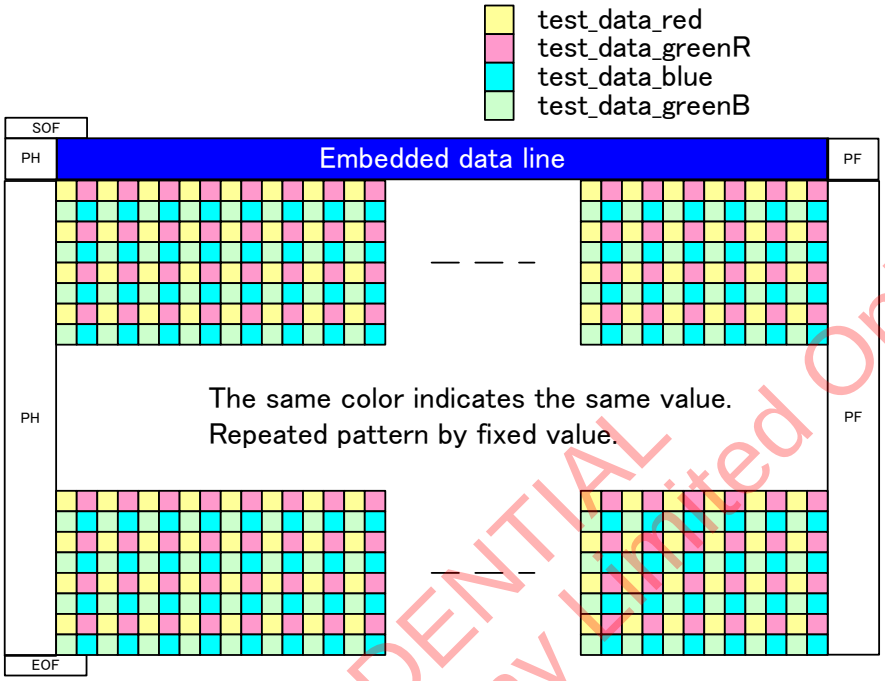
Address	Name	Description
0x0600	test_pattern_mode	0 – no pattern (default)
0x0601		1 – solid color
		2 – 100 % color bars
		3 – fade to grey color bars
		4 - PN9
0x0602	test_data_red	The test data used to replace red pixel data
0x0603		
0x0604	test_data_greenR	The test data used to replace green pixel data on rows that also have red pixels
0x0605		
0x0606	test_data_blue	The test data used to replace blue pixel data
0x0607		
0x0608	test_data_greenB	The test data used to replace green pixel data on rows that also have blue pixels
0x0609		
0x060A	horizontal_cursor_width	Defines the width of the horizontal cursor (in pixels)
0x060B		

Address	Name	Description
0x060C	horizontal_cursor_position	Defines the top edge of the horizontal cursor
0x060D		
0x060E	vertical_cursor_width	Defines the width of the vertical cursor (in pixels)
0x060F		
0x0610	vertical_cursor_position	Defines the left hand edge of the vertical cursor. A value of 0xFFFFswitches the vertical cursor into automatic mode where it automatically advances every frame.
0x0611		

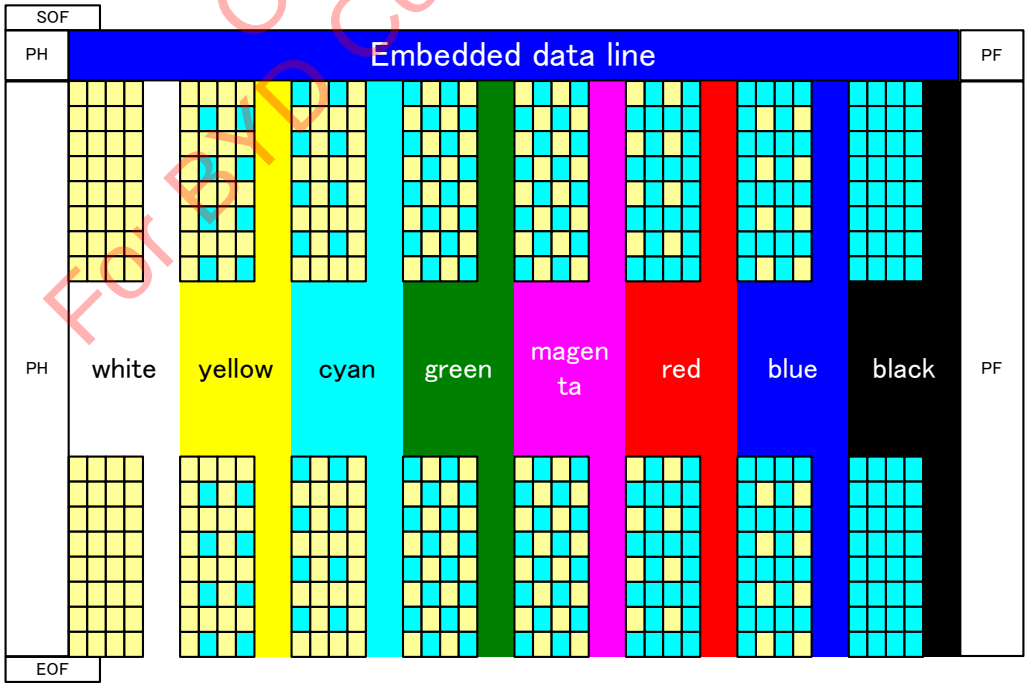
6-1.1.1 Pattern Description

Table. 24 Description of Test Patterns

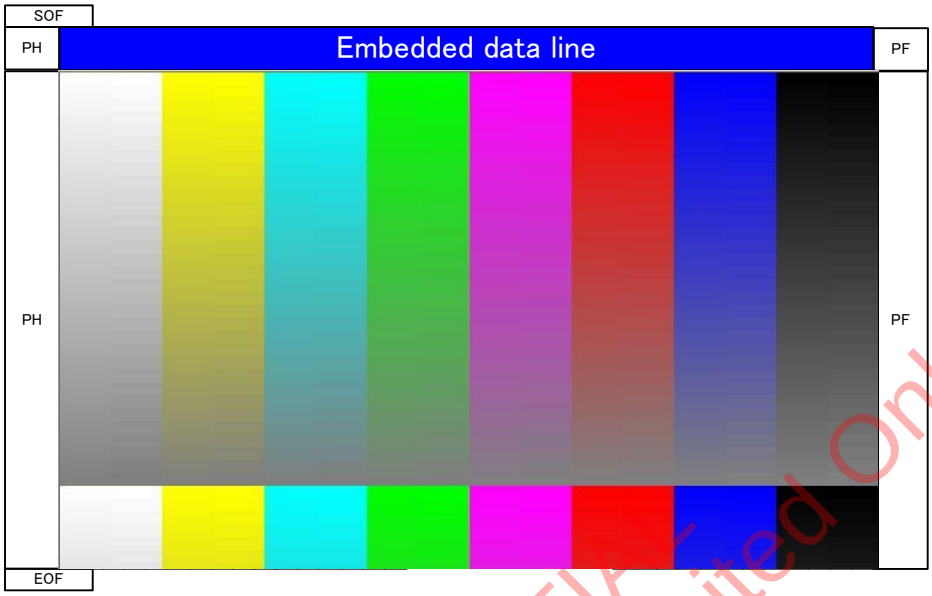
Solid Colour
test_pattern_mode = 1
test_data_red/test_data_greenR/test_data_blue/test_data_greenB = Arbitrary value



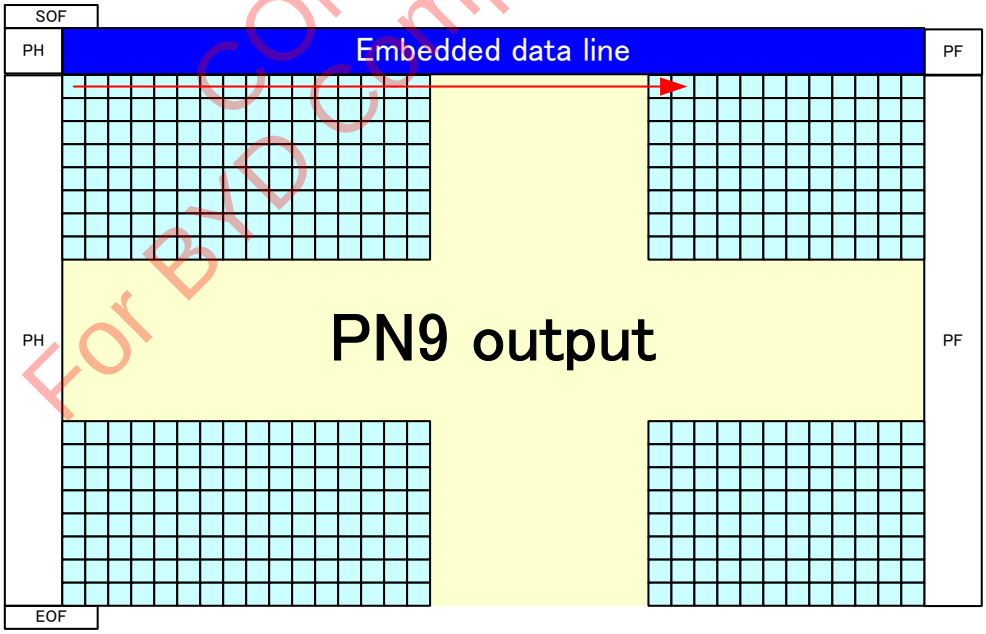
100 % colour bars
test_pattern_mode = 2



Fade to grey colour bars
test_pattern_mode = 3



PN9 (512 bit pseudo-random data)
test_pattern_mode = 4



PN9 is generated by the generator polynomial of $X^9 + X^5 + 1$ as the initial value = 1

6-2 Digital Gain Setting

See section 5-7.2 Digital gain settings.

6-3 Black Level Adjust

The register required to set the Black Level Adjust is as follows.

Table. 25 Black Level Adjust Setting Register

Index (HEX)	Bit	Register Name	RW	Comment	Re-Timed	Default (HEX)
300B	[7:0]	BLKLEVEL	RW	Set Black Level		40
30E5	[11]	Blklevel_set (testdi[11])	RW	Defines pedestal level. 0: pedestal = 0x40 (fixed) 1: pedestal = BLKLEVEL		0

6-4 Defect Correction

The registers required to set the Defect Correction are as follows.
3 different functions are implemented;

1. Dynamic single defect pixel correction
2. Static same color adjoin pixel correction
3. Static 2x4 defect pixel correction

Defect addresses for mapped_couplet_correct (couplet defect: two adjacent defect pixels of the same color) are stored in NVM (see section7-5), and sensor processes them in itself.

Table. 26 Defect Correction Setting Registers

Index (HEX)	Bit	Register Name	RW	Comment	Re-Timed	Default (HEX)
4100	[2]	ZNR_FD_DFCT_SW	RW	0: Static Mode Off 1: Static Mode On	V-Sync	0 (*)
4100	[5:3]	ZNR_DIFF_DFCT_SW	RW	[3]: Dynamic Mode-1 [4]: Dynamic Mode-2 [5]: Dynamic Mode-3	V-Sync	1
4102	[4:0]	ZNR_Coefficient1	RW	Parameter Setting1		A
4103	[7:0]	ZNR_Coefficient2	RW	Parameter Setting2		00
4104	[6:0]	ZNR_Coefficient3	RW	Parameter Setting3		32
4105	[6:0]	ZNR_Coefficient4	RW	Parameter Setting4		32
4106	[6:0]	ZNR_Coefficient5	RW	Parameter Setting5		40
4107	[6:0]	ZNR_Coefficient6	RW	Parameter Setting6		40

(*) 4100[2] is recommended to be set 1.

6-5 Pixel Re-alignment H Direction

The registers required to set the Pixel Re-alignment H Direction are as follows.

Table. 27 Pixel Re-alignment H Direction Setting Registers

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0344	[3:0]	X_ADD_STA[11:8]	RW	x_addr_start	V sync	0	
0x0345	[7:0]	X_ADD_STA[7:0]	RW		V sync	00	
0x0348	[3:0]	X_ADD_END[11:8]	RW	x_addr_end	V sync	0C	
0x0349	[7:0]	X_ADD_END[7:0]	RW		V sync	CF	
0x0390	[1:0]	BINNING_MODE	RW	defines binning mode. 0:no-binning 1:2x2-binning 2:4x4-binning	V sync	0	

6-6 Scaling

The registers required to set the Scaling are as follows.

Table. 28 Re-sizing Setting Registers

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL
0x0400	—						
0x0401	[1:0]	Scaling_mode	RW	0 – No scaling, 1 – Horizontal Scaling, 2 – Full Scaling (both H and V)	V sync	00	○
0x0404	[0]	scale_m	RW	Down scale factor: M component Range: (16d< = scale_m< = 256d) upwards Format: 16-bit unsigned integer	V sync	0	○
0x0405	[7:0]					10	○
0x0407	[4:0]	scale_n	RO	Down scale factor: N component Value: 16 (fixed) Format: 16-bit unsigned integer		10	○

7. NVM Memory Map

7-1 Block Diagram

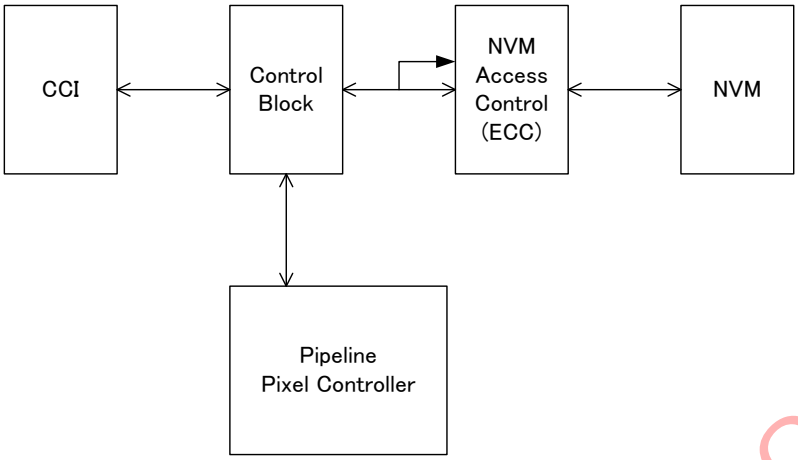


Fig. 34 Block Diagram

NVM is composed of 16 pages (from 0 to 15) and 64 bytes per page. ECC is also applied for every 16 address (bytes), 4 rows in 1 page.

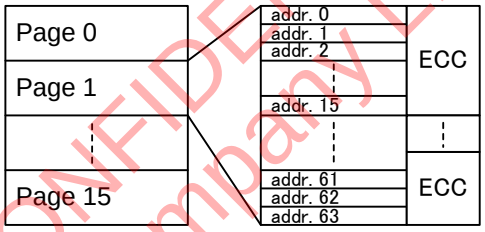


Fig. 35 NVM Map structure

7-2 NVM Functions

NVM block has following functions.

Table. 29 Functions via NVM

No	Item	Description
1	Data Interface	User can write/read data via CCI by the unit of page
2	Writing Reg. Value	Writing assigned address and values which are transferred into the assigned registers.
3	Writing Defect address	Writing assigned address, whose values are used for defect corrections
4	Reading	Reading NVM data by the unit of page, not ECC region
5	ECC Function	Can apply ECC for each 16 bytes (1-row) block. 1-bit per 16 bytes can be corrected.
6	ECC status	Can check while reading/writing that ECC is applied by page. 1. Read data is correct. No ECC is applied. 2. Read data is correct with 1-bit correction of ECC. 3. Read data is incorrect though ECC is applied (means >2 bits per a unit of 16-byte (row) are incorrect).

7-3 Related Registers

Registers to be related about NVM are the followings.

Table. 30 Related Registers

Index	Byte	Register Name	RW	Comment	Re-Time	Default (HEX)	Embd DL	Comments
0100	[0]	Mode_sel	RW	Mode select 0: SW- Standby 1: Streaming		0		
3380	[7:0]	SYSOTP_IF_MODE1	RW	OTP mode setting [1:0]:control access cycle to fuse cell 00:INCK cycle 01:INCK/2 cycle 10:INCK/4 cycle [3]:ECC disable switch 0:ECC on,1:ECC off [5]:write mode; 0: test mode 1: recommended		00		
30CC	[7:0]	TESTTGCU	RW	Monitor Output		00		
301B	[2:0]	FSTROBESEL	RW	Set FStrobe pin to monitor		00		
3368	[15:8]	INCK_FREQ[15:8]	RW	input_clk_frequency_mhz (need input)		0B		
3369	[7:0]	INCK_FREQ[7:0]	RW			6E		
3382	[15:8]	SYSOTP_IF_WRCNT[15:8]	RW	OTP write clock setting		07		
3383	[7:0]	SYSOTP_IF_WRCNT[7:0]	RW			80		
3400	[2:0]	OTPIF_CTRL	RW	OTP I/F control register [0] enable [1]R/W [2]error clear		00		
3401	[1:0]	OTPIF_STATUS	RO-D	OTP I/F status; [0] ready [1] error		00		
3402	[2:0]	OTPIF_PAGE_SELECT	RW	otpif_page_select		00		
3404	[7:0]	OTPIF_DT_0	RW	otpif_data_0		00		
(DT_1 to DT_62)								
3443	[7:0]	OTPIF_DT_63	RW	otpif_data_63		00		Trigger to start write sequence
5801	[5:4]		RO	00: No data error exists. 01: Data error and corrected by ECC. = Read data is correct. 11: Data error exists, and cannot be corrected by ECC. Read data is incorrect.		00		

Before writing / reading following steps are required

0. Set Sensor being SW-Standby by 0x0100 = 0h
1. Set monitor output to check writing pulse. (option, debug purpose only)
2. Set OTP write clock setting.
(When INCK = 9 MHz, 021Ch at 0x3382, 0x3383)
3. Set clock frequency that user supplies to the sensor.
(When INCK = 9 MHz, 0900h at 0x3368, 0x3369)

Then when writing;

1. Set controller "ECC ON" or ECC OFF" by 0x3380 = "20h" (ECC ON) or "28h" (ECC OFF)
2. Set Write by 0x3400 = "3h."
3. Set page from 0 to 12 by 0x3402.
4. Set 0x3404 to 0x3443 OTPIF_DT_0to 63 = xxh (Data to Write) *1
5. Set again OTPIF_DT_63 with the same value that one sets in previous section. (4)

Then when reading;

1. Set controller “ECC ON” or “ECC OFF” by 0x3380 = 00h (ECC ON), 08h (ECC OFF)
2. Set Read by 0x3400 = "1h."
3. Set page from 0 to 12 by 0x3402.
4. Set 0x3404 to 0x3443 OTPIF_DT_0to 63 = xxh (Data to Write)

*1 Since OTP write data are once stored into “Buffer memory”, whole page data including no-write data = “0x00” must be set via CCI to calculate error correction codes. And if there are any written pages with ECC_OFF, same date value must be written. When final writing, it should be written with ECC_ON.

7-4 Manuals

Due to ECC applied to NVM data, following steps are required during writing and reading.

7-4.1 Writing Sequence

1st step is Initial read check to sort out initial failure

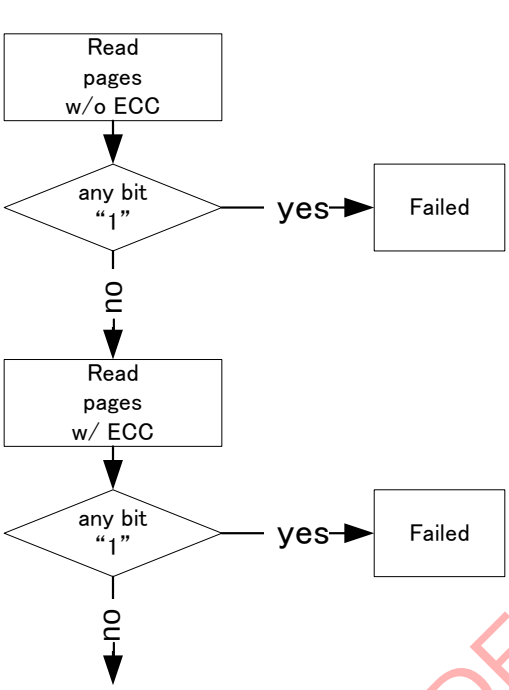


Fig. 36 Flow chart for initial Reading

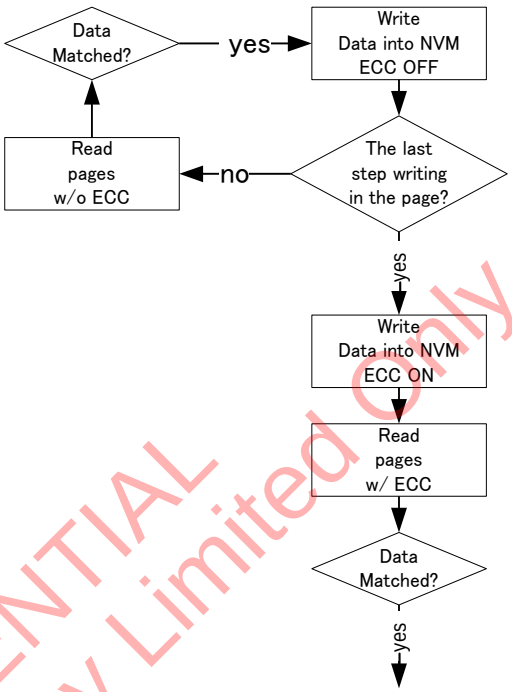


Fig. 37 Flow chart for Multi step Writing

After this check, write sequence can start as followings.

Table. 31 Example of multi-step writing in the page w/ ECC function

Page	Addr	1st	2nd		The Last
X	000	A			A
X	001		B		B
X					
X	015			C	C
X	016			D	D
X					
X	063			E	E
0x3380		28h	28h	28h	20h

The table shows example of multi-step writing in one page w/ ECC function. Integrators need to turn on ECC at the last writing to secure NVM writing.

7-4.2 Reading Sequence

When reading NVM, ECC ON/OFF needs to be matched in the last writing. Followings are the example settings.
ECC OFF; 0x3380 = 08h
ECC ON; 0x3380 = 00h

7-5 NVM Memory Map

Table. 32 NVM Memory Map Example

Page (dec)	Row (dec)	addr (hex)	Category	Name	value (hex)	data Owner
0	0-3	000 -03F	Reserved			Integrator
1	4-7	040 -07F	Reserved			Integrator
2	8-11	080 -0BF	Reserved			Integrator
3	12-15	0C0 -0FF	Reserved			Integrator
4	16-19	100 -13F	Reserved			Integrator
5	20-23	140 -17F	Reserved			Integrator
6	24-27	180 -1BF	Reserved			Integrator
7	28-31	1C0 -1FF	Reserved			Integrator
8	32-35	200 -23F	Reserved			Integrator
9	36-39	240 -27F	Reserved			Integrator
10	40-43	280 -2BF	Reserved			Integrator
11	44-47	2C0 -2FF	Reserved			Integrator
12	48-51	300 -33F	Reserved			Integrator
13	52-55	340 -37F	please don't write			Sony
14	56-59	380 -3BF	please don't write			Sony
15	60-63	3C0 -3FF	please don't write			Sony

8. Other Functions

8-1 Clock System

8-1.1 Clock Structure

The IMX179 clock system has the following structure.

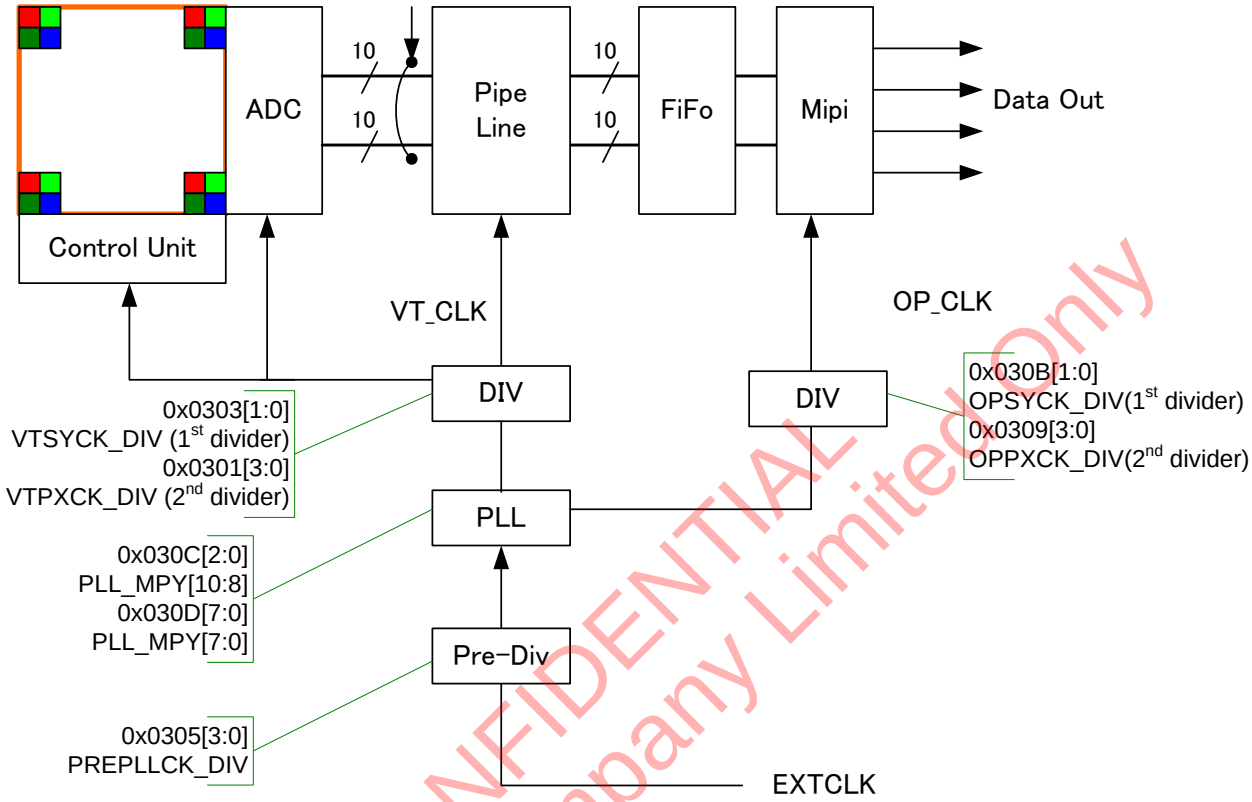


Fig. 38 Clock System Block Diagram

The IMX179 is comprised of 2 ch Pipe-Line, and 1 PLL for both pixel read domain and Output data domain.

9. Electrical Characteristics

9-1 Absolute Maximum Ratings

Table. 33 Absolute Maximum Ratings

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage (analogue)	V_{ANA}	-0.3		3.3	V	
Supply voltage (Core)	V_{DDL}	-0.3		2.0	V	
Supply voltage (IF)	V_{DIG}	-0.3		3.3	V	
Input voltage	V_I	-0.3		3.3	V	
Output voltage	V_O	-0.3		3.3	V	
Operating temperature	Topr	-20		+60	˚C	Tj
Storage temperature	Tstg	-30		+80	˚C	Tj
Performance guarantee temperature	Tspec	-20		+60	˚C	Tj

9-2 Recommended Operating Conditions

Table. 34 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage (analogue)	V_{ANA}	2.6	2.7	2.9	V	Performance limit
		2.4				Functional limit
Supply voltage (Core)	V_{DDL}	1.1	1.2	1.3	V	
Supply voltage (IF)	V_{DIG}	1.62	1.8	1.98	V	

9-3 Electrical Characteristics

Table. 35 DC Characteristics

Item	Pins	Symbol	Min.	Typ.	Max.	Unit	Comment
Supply voltage	VDDSUBD	V_{ANA}	2.6 *1 2.4 *2	2.7	2.9	V	*1; performance limit *2; functional limit
	VDDHCP						
	VDDHCM1,2						
	VDDHAN						
	VDDHPL						
	VDDHSN1-3						
	VDDMCO	V_{DIG}	1.62	1.8	1.98	V	Need Evaluation to fit requirements
	VDDLSC1-4	V_{DDL}	1.1	1.2	1.3	V	
	VDDLCN1,2						
	VDDLIO1,2						

Item	Pins	Symbol	Min.	Typ.	Max.	Unit	Comment
Digital input/output voltage	SCL, SDA	VIL	-0.5		0.3VDIG	V	
		VIH	0.7VDIG		VDIG + 0.5	V	
		VOL			0.25VDIG	V	for currents abs (2 mA)
		VOH	0.75VDIG			V	for currents abs (2 mA)
Digital output voltage	REGEN GPIO 1,2,3,4	VOL			0.45	V	
		VOH	VDIG-0.45			V	
Digital input voltage	INCK XCLR	VIL	-0.3		0.35VDIG	V	
		VIH	0.65VDIG		VDIG + 0.3	V	

9-4 AC Characteristics

9-4.1 Master Clock Waveform Diagram

9-4.1.1 INCK Square Waveform Input Specifications

Input specifications are shown below when square-wave inputs directly into the external pin INCK.

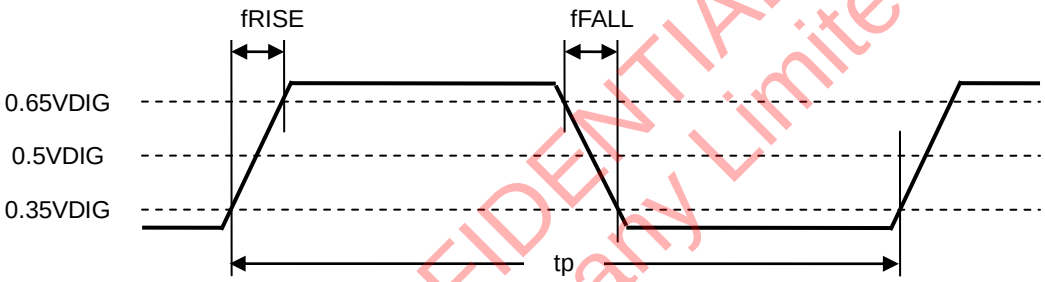


Fig. 39 Master Clock Square Waveform Diagram

Table. 36 Master Clock Square Waveform Input Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Comment
Frequency	fSCK	6	18	27	MHz	
jitter (period, peak-to-peak)	Tjitter			600	ps	
Rise Time	fRISE	1		10	ns	
Fall Time	fFALL	1		10	ns	
Duty Cycle	fDUTY	45		55	%	
Input Leakage	fILEAK	-10		10	µA	

9-5 Electrical Characteristics

Table. 37 Electrical Characteristics

(V_{ANA} = 2.9 V, V_{DDL} = 1.2 V, V_{DIG} = 1.92 V, Tj = 60 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Comment
Current consumption (15 frame/s)	IVAVA_strm			48	mA	VTmax is max speed read out from pixel array CSI2 4 lanes
Current consumption (30 frame/s, 2x2 bin)				48	mA	
Current consumption (VTmax)				48	mA	
Current consumption (15 frame/s)	IVDIG_strm			1	mA	VTmax is max speed read out from pixel array CSI2 4 lanes
Current consumption (30 frame/s, 2x2 bin)				1	mA	
Current consumption (VTmax)				1	mA	
Current consumption (15 frame/s)	IVDDL_strm			130	mA	VTmax is max speed read out from pixel array CSI2 4 lanes
Current consumption (30 frame/s, 2x2 bin)				130	mA	
Current consumption (VTmax)				200	mA	
HW-Standby current (ttl)	ISTB			10060	µA	V_{DDL} shall be disabled
HW-Standby current (analog)	ISTB_ana			50	µA	
HW-Standby current (if)	ISTB_dig			10	µA	
HW-Standby current (digital)	ISTB_ddl			10000	µA	V_{DDL} shall be disabled

Note) Measurement conditions

10. Image Sensor Characteristics

10-1 Spectral Sensitivity Characteristics

(Excluding lens characteristics and light source characteristics)

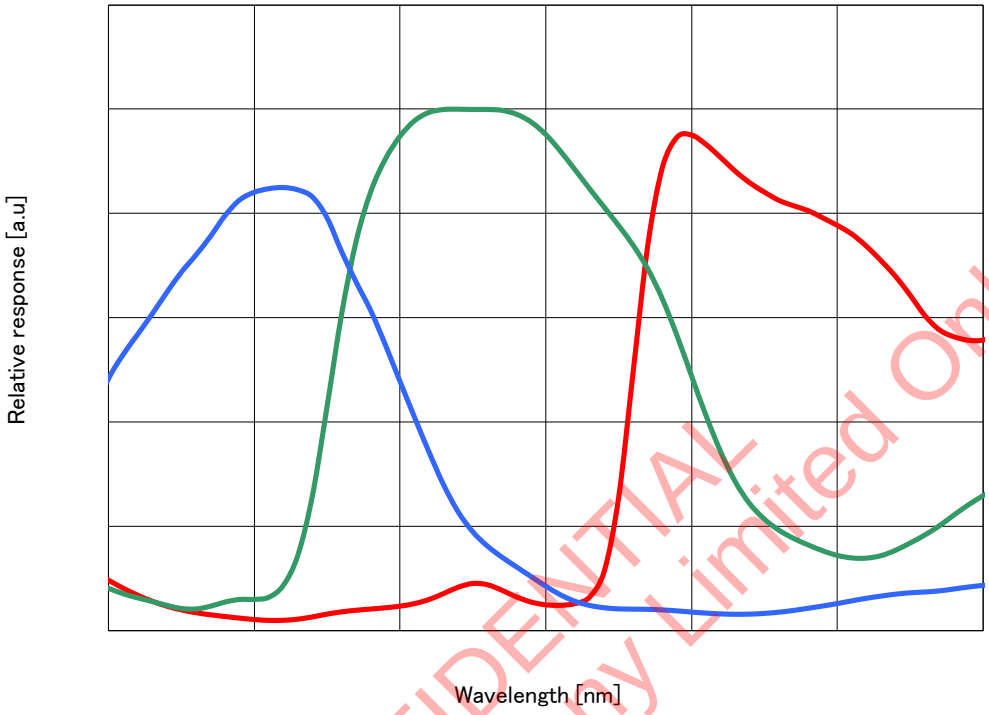


Fig. 40 Example of Spectral Sensitivity Characteristics

10-2 Image Sensor Characteristics

Table. 38 Image Sensor Characteristics

(V_{ANA} = 2.7 V, V_{DDL} = 1.2 V, V_{DIG} = 1.8 V, Tj = 60 °C, Typical Gain (0 dB))

Item	Symbol	Min.	Typ.	Max.	Unit	Range	Measure-ment method	Remarks
Sensitivity	S	310			LSB (*1)	Center	ISC_1	1/120 s storage
Sensitivity ratio	RG	39.0	46.0	53.0	%	Zone0	ISC_2	1/15 s storage
	BG	42.0	49.0	56.0				
Saturation signal	Vsat	959			LSB	Zone0	ISC_3	1/15 s storage
Dark signal	Vdt			0.5	LSB	Zone2D	ISC_4	1/30 s storage

(*1) LSB is abbreviation of Least Significant Bit, and it indicates signal output unit when 10bits = 1023 digital output.

10-3 Spot Pixel Specifications

Table. 39 Spot Pixel Specifications

(15 frame/s, V_{ANA} = 2.7 V, V_{DDL} = 1.2 V, V_{DIG} = 1.8 V, Tj = 60 °C)

Type of distortion	Level Note 1)	Maximum distorted pixels in Zone2D	Measurement method	Remarks
2x4 defect in the dark	405 LSB ≤ D	15 address (*1)		18 dB gain
2 same color adjoin at high light	19 % < |D|	5 (total) (*1)		
2 same color adjoin at dark	405 LSB ≤ D			18 dB gain
Black or white pixel at high light	19 % < |D|	Total 1000ppm for each color plane	SPS_1	
White pixels in the dark	405 LSB ≤ D		SPS_2	18 dB gain
3 or more same color adjoin at high light	19 % < |D|	0		
3 or more same color adjoin at dark	405 LSB ≤ D			18 dB gain

(*1) These defects will be corrected by internal static defect correction.

Note1) D...Spot pixel level.

Note2) The above chart (hereinafter referred to as the “White and Black Pixel Specifications”) is the standard only for sorting CMOS image sensor products in this specification book (hereinafter referred to as the “PRODUCTS”) before shipment from a manufacturing factory. Sony Corporation and its distributors (collectively hereinafter referred to as the “Seller”) disclaim and will not assume any liability even if actual number of distorted pixels of the PRODUCTS delivered to you exceeds the maximum number set forth in the White and Black Pixel Specifications. You are solely liable for any claim, damage or liability arising from or in connection with such distorted pixels. If the Seller separately has its own product warranty program for the PRODUCTS (the “Program”), the conditions in this specification book shall prevail over the Program and the Seller shall not assume any liability under the Program to the extent there is contradiction.

10-4 Zone Definition

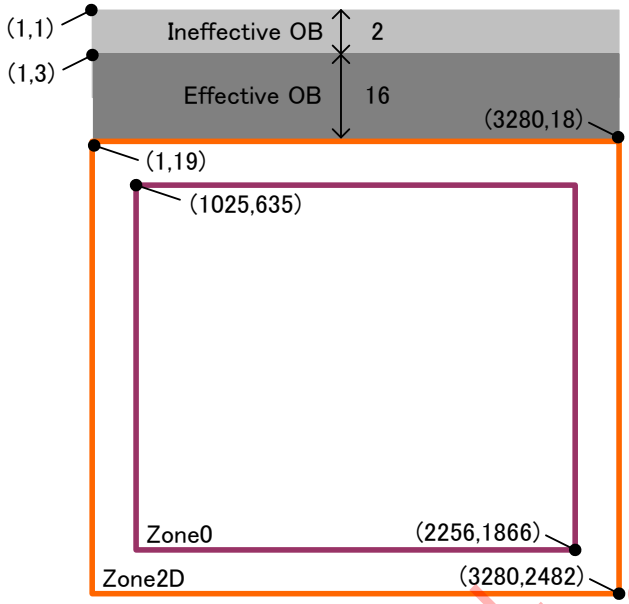


Fig. 41 Zone Definition Diagram

10-5 Image Sensor Characteristics and Spot Pixel Measurement Method

10-5.1 Measurement conditions

The device drive conditions are at the typical values of the bias and clock voltage conditions.

Table. 40 Measurement Conditions

Supply voltage	Analogue 2.7 V, digital 1.2 V, IF 1.8 V
Clock	INCK 9 MHz

In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

10-5.2 Color coding of this image sensor & Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.
All pixel signals are output successively in a 1/15 s period.

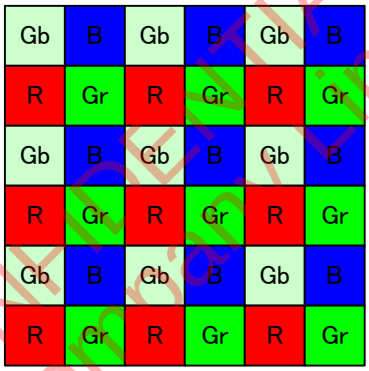


Fig. 42 Color Coding Diagram

10-5.3 Definition of standard imaging conditions

10-5.3.1 Standard imaging condition I

Use a pattern box (luminance: 706 cd /m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

10-5.3.2 Standard imaging condition II

A testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or storage time control by the electronic shutter.

10-5.3.3 Standard imaging condition III

IA testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output or storage time control by the electronic shutter.

Image sensor characteristics measurement method

ISC_1. Sensitivity

Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/120 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

$$S = \frac{VGr + VGb}{2} \text{ [LSB]}$$

ISC_2. Sensitivity ratio

Set the measurement condition to the standard imaging condition II. After adjusting so that the average value of the VG signal output is 430[LSB], measure the R signal output (VR [LSB]), the Gr and Gb signal outputs (VGr, VGb [LSB]) and the B signal output (VB [LSB]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

$$VG = \frac{VGr + VGb}{2}$$

$$RG = \frac{VR}{VG}$$

$$RB = \frac{VB}{VG}$$

ISC_3. Saturation signal

Set the measurement condition to the standard imaging condition III. After adjusting the luminous intensity to 20 times the intensity with the average value of the G signal output, 430[LSB], measure the average value of the Gr, Gb, R and B signal outputs.

ISC_4. Dark signal

Measure the average value (Vdt[LSB]) of the signal output in zone2D in the light-obstructed state.
Define the average value of the signal output accumulated in 1 frame period (tlv) as Vdt1V and the average value of the signal output accumulated in the shortest period (1H period: tlh) as Vdt1H, and then substitute the values into the following formula.

$$Vdt = (Vdt1V - Vdt1H) / (t1v - t1h) / 30 \text{ [LSB]}$$

10-5.4 Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after if you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of storage time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
16 LSB or higher	1.7 pcs
29 LSB or higher	1.1 pcs
71 LSB or higher	0.6 pcs
147 LSB or higher	0.3 pcs
212 LSB or higher	0.3 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

10-5.5 Measurement Method for Spot Pixels

Measure under the standard imaging condition II.

SPS_1. Black or white pixels at high light

After adjusting the average value of the Gr/Gb signal output to 430[LSB], measure the local dip point (black pixel at high light, V_{XB}) and peak point (white pixel at high light, V_{XK}) in the Gr/Gb/R/B signal output V_X (x = Gr/Gb/R/B), and substitute the values into the following formula.

$$D_K(\text{WhitePixellevel}) = \frac{\overline{V_{XK}}}{\overline{V_X}} \times 100[\%]$$

$$D_B(\text{Blackpixellevel}) = \frac{\overline{V_{XB}}}{\overline{V_X}} \times 100[\%]$$

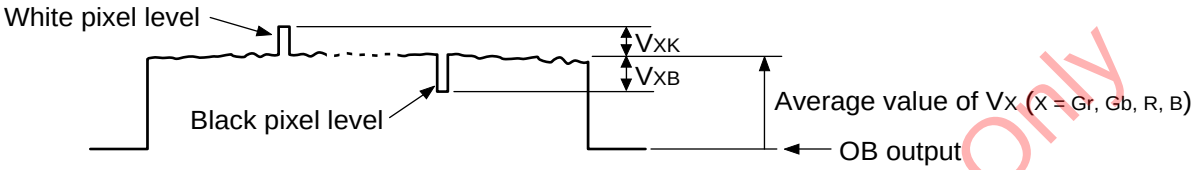


Fig. 43 Measurement Method for Spot Pixels

SPS_2. White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

11. Chief Ray Angle Characteristics

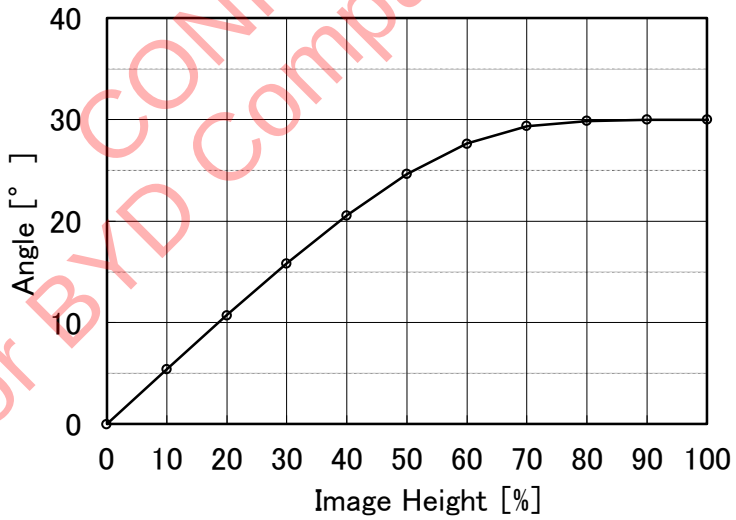


Fig. 44 Chief Ray Angle

12. Connection Example

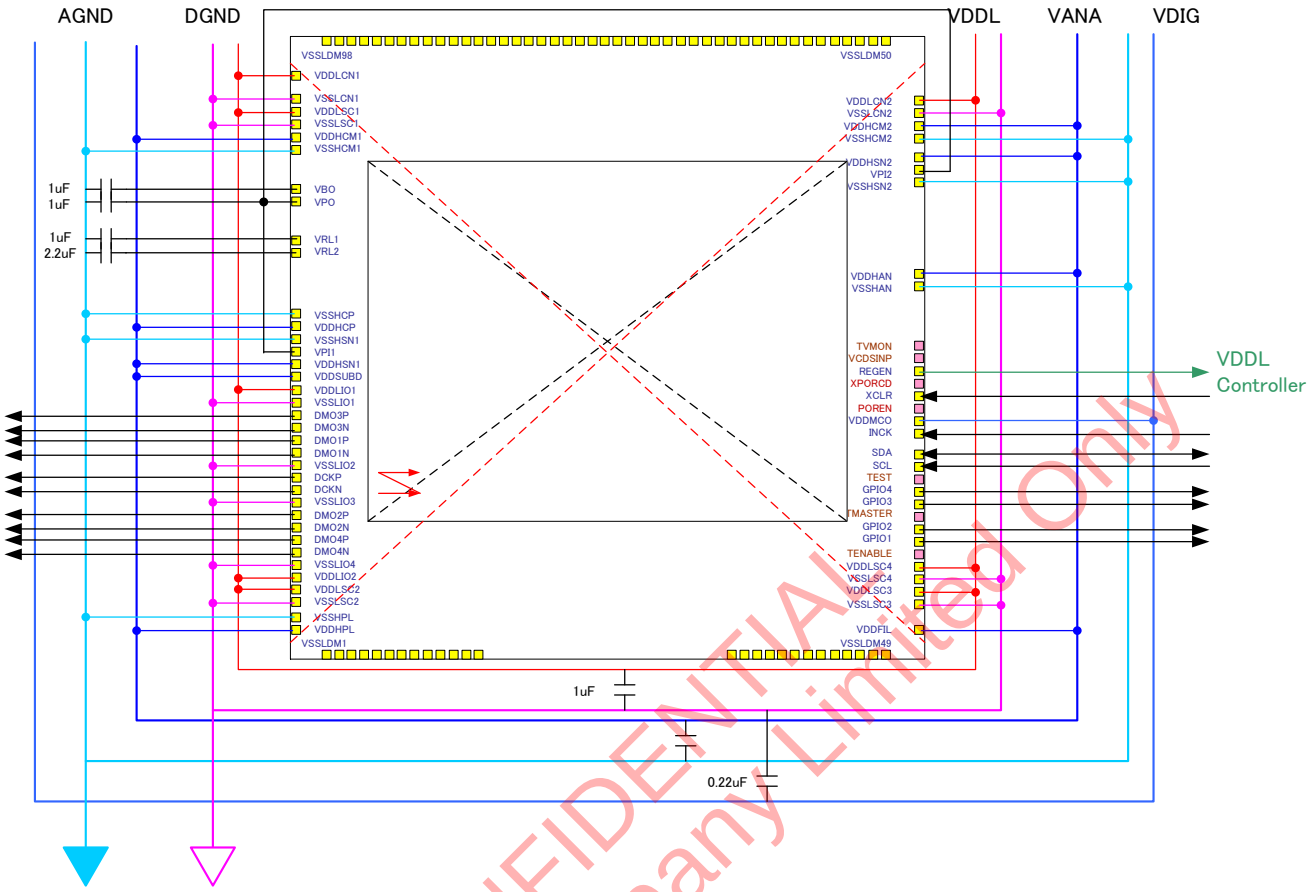


Fig. 45 Recommended Circuit

Note) When fixing the voltage of chip back side, fix it to VDDSUBD voltage

13. Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

(1) Perform all work in a clean environment.
(2) Do not touch the chip surface with hand and make any object contact with it.
(3) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

3. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Reliability assurance of this product should be ignored because it is a bare chip.
(5) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(6) Note that X-ray inspection may damage characteristics of the sensor.
(7) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.
(8) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.